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MS-7816

Intel -SharkBay plamform Z87

ATX

Ver: 10(243.84x304.8)

CPU:

Haswell LGA1150

System Chipset:

Lynx Point Z87

Onboard Chip:

HD Audio Codec:ALC892

LAN-RTL8111E

SIO:Nuvoton 6779D

Flash ROM: SPI 64 MB & SPI 128 MB (H87&B85)

Main Memory:

DDRIII (1066/1333/1600MHz) * 4 (Dual Channel)

ACPI:

UP1

PWM:

UP1649 6 Phase

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

PCI Express (X4) Slot * 1

PCI Slot * 3

Other:

SATA3.0 x6(PCH)

REAL USB2.0 *6

FRONT USB2.0 *4(B85 Disable 2 port)

REAL USB3.0 *2

FRONT USB3.0 *2

MS-7816 Block Diagram

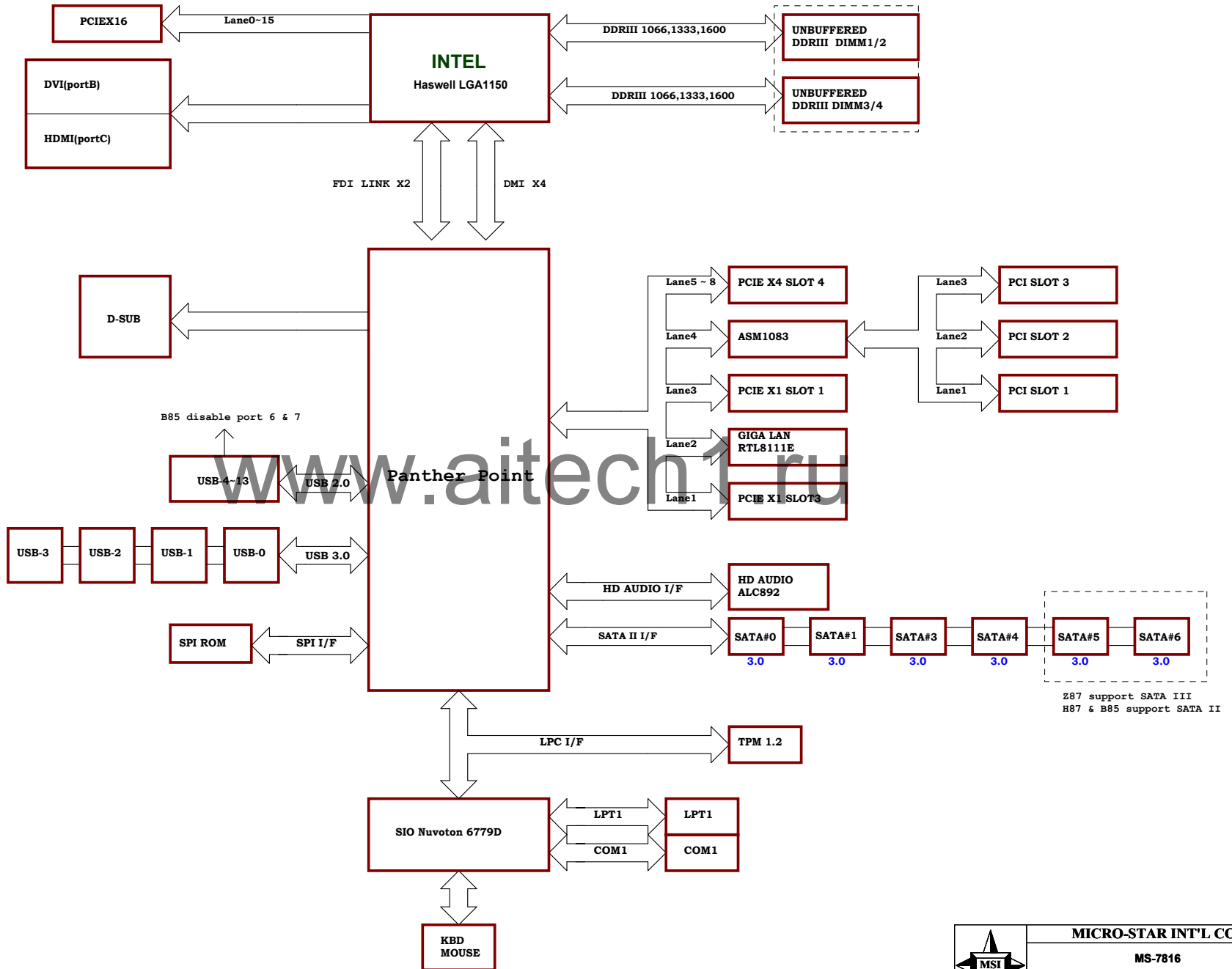
**Slot Sequence:**

Diagram illustrating the configuration of a 16-lane PCIe slot:

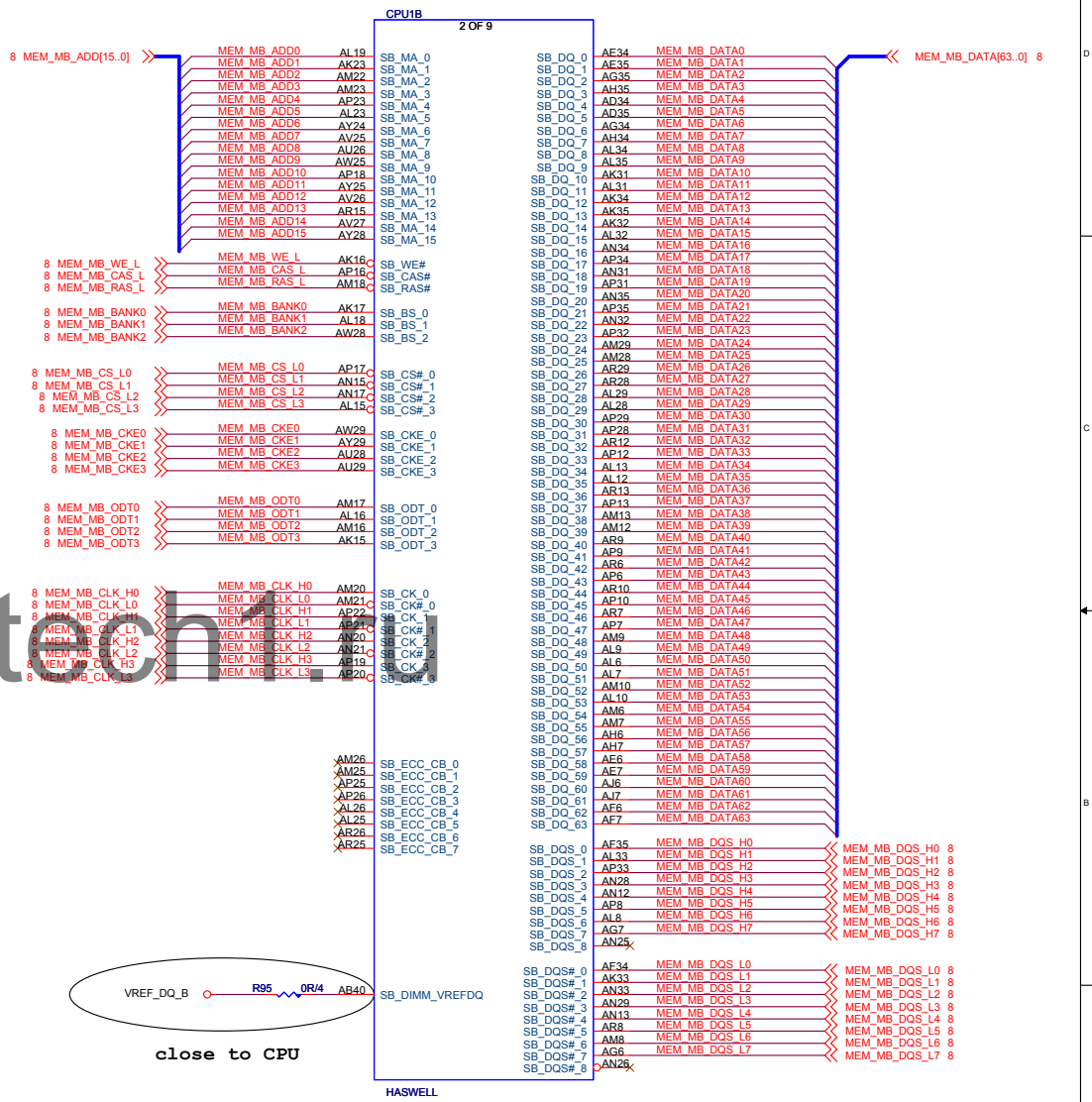
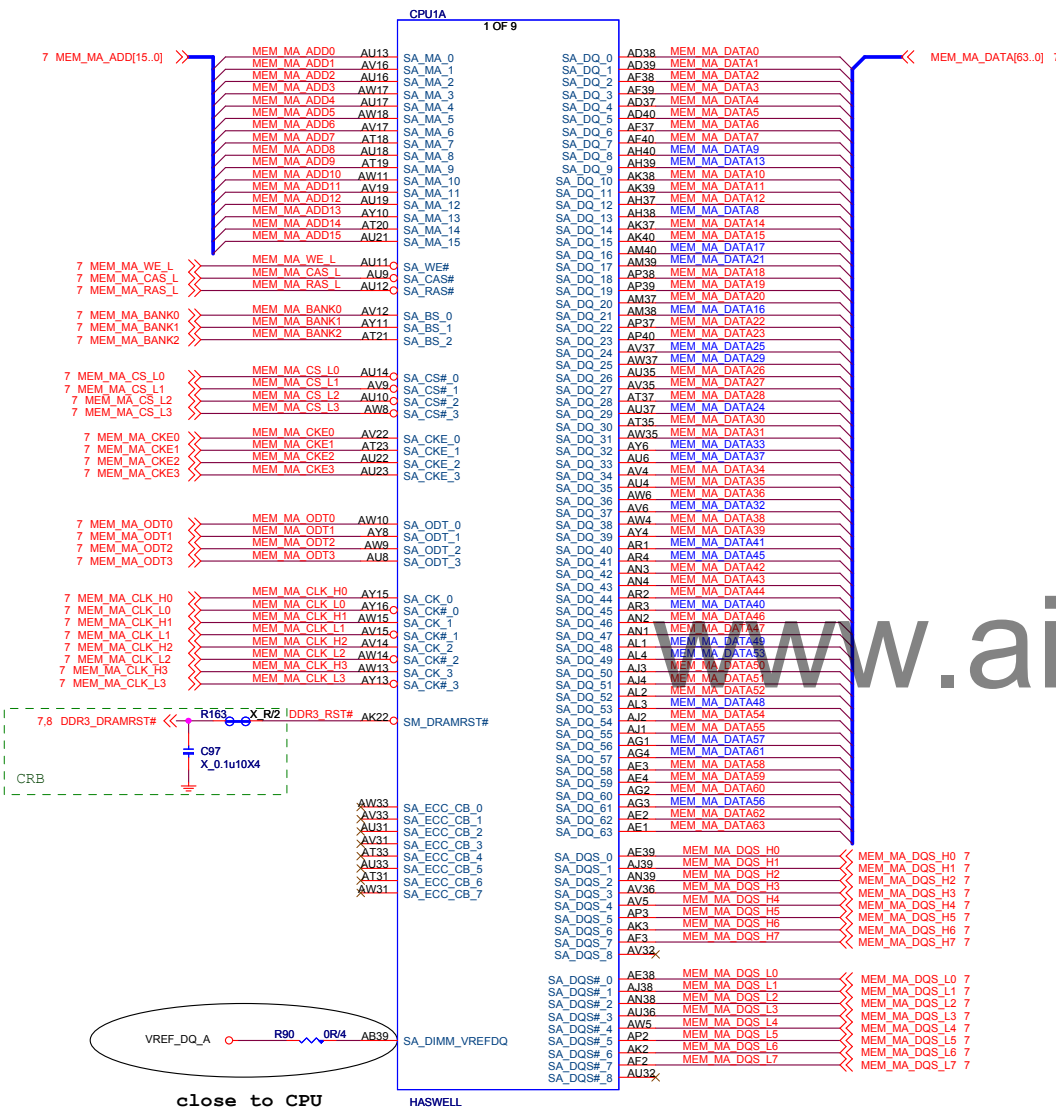
- Top section: PCIe X1 (1 lane) and PCIe X16 (16 lanes)
- Second section: PCIe X1 (1 lane) and PCI SLOT (1 lane) and PCIe X16(X4) (4 lanes)
- Third section: PCI SLOT (1 lane)
- Bottom section: PCI SLOT (1 lane)

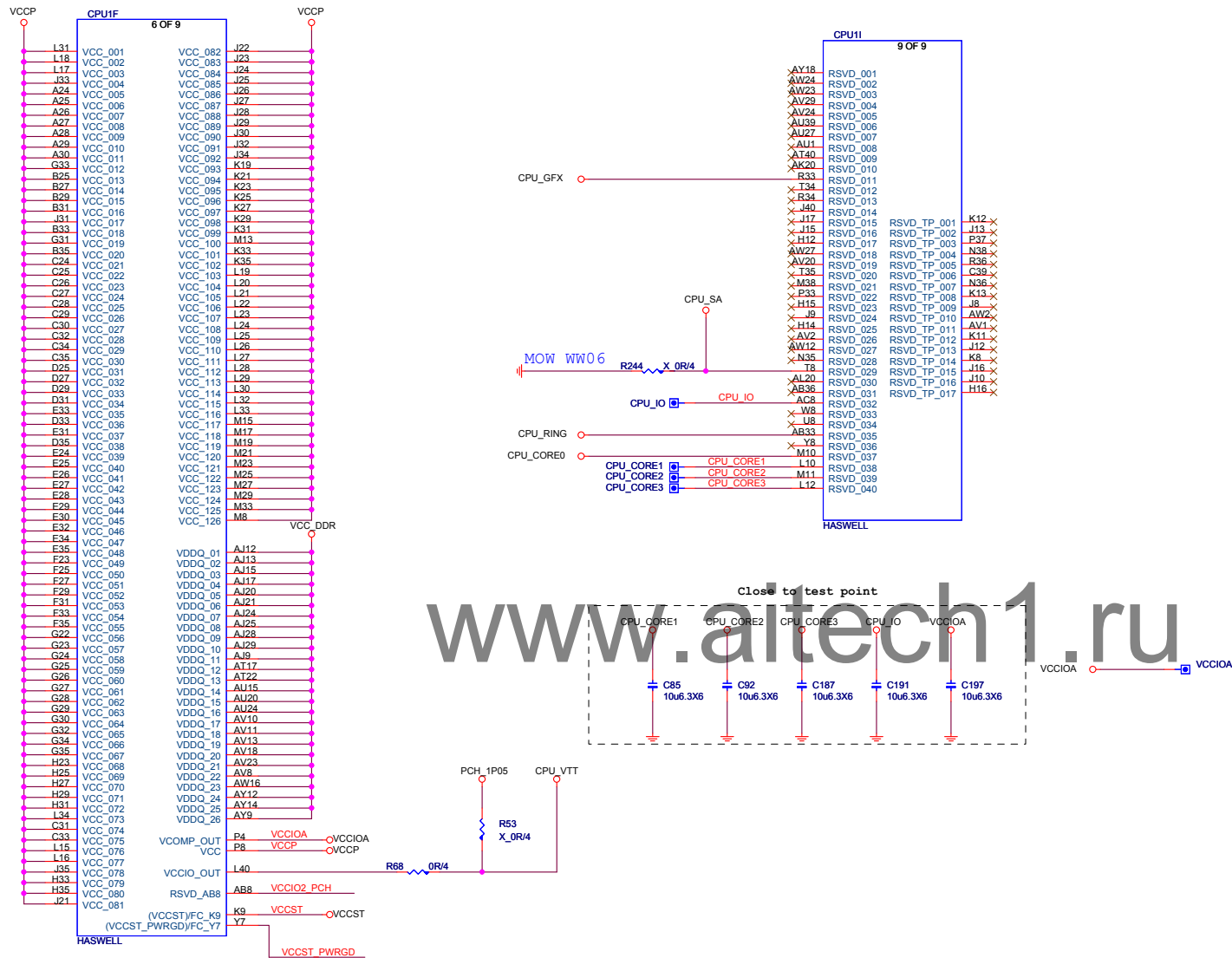


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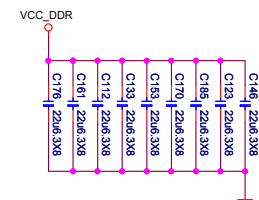
MS-7816

Size Custom	Document Description Block Diagram	Rev 10
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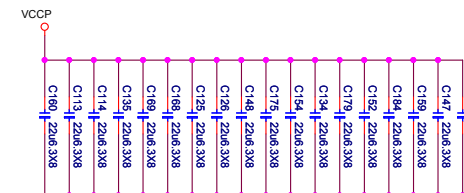


+1.5V_DDR3-Decoupling



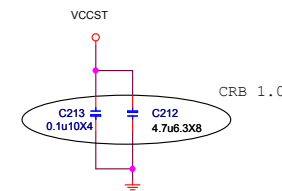
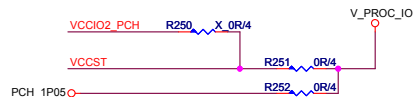
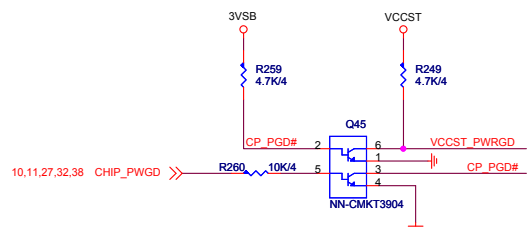
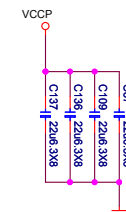
CPU SOCKET CAVITY 0805CAPS

+CPU_VCCP-Decoupling



PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

PLACE 0805CAPS Near CPU SOCKET edge

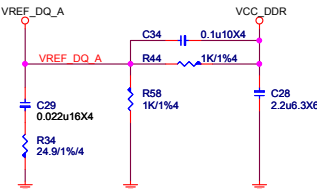


MICRO-STAR INT'L CO.,LTD

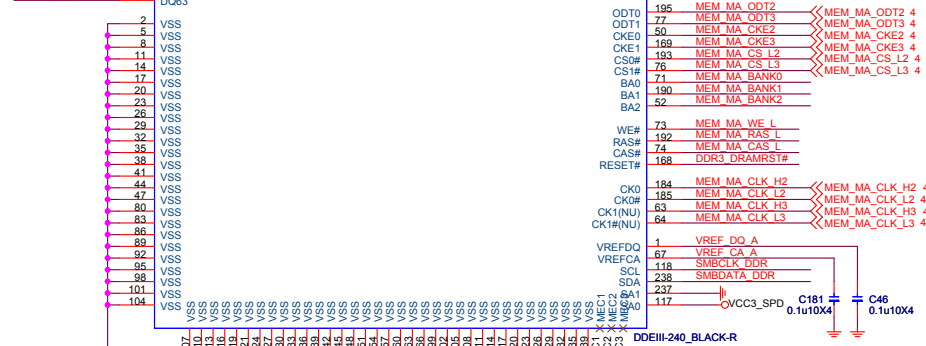
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Size	Document Description	Rev
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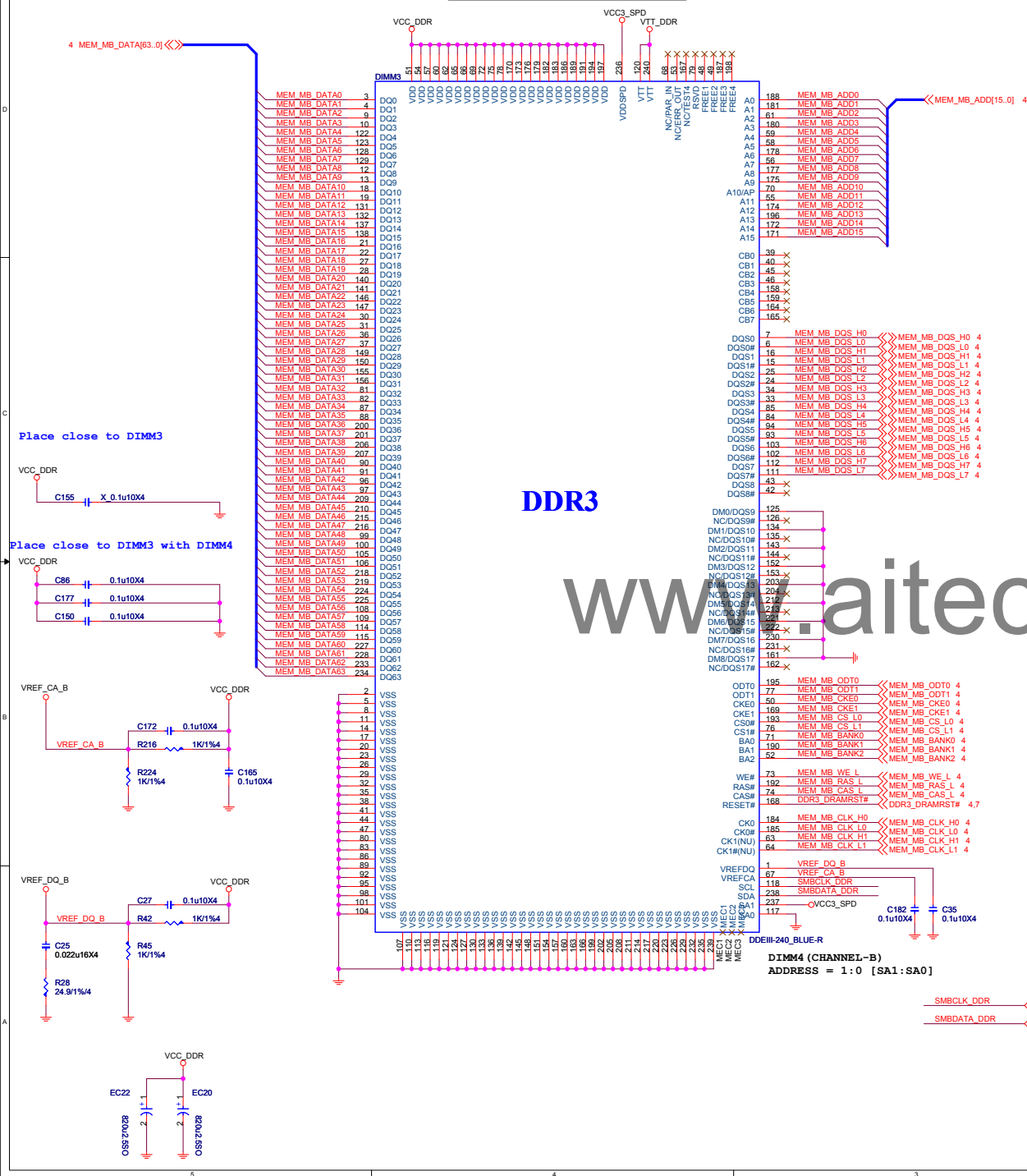


DDRIII DIMM

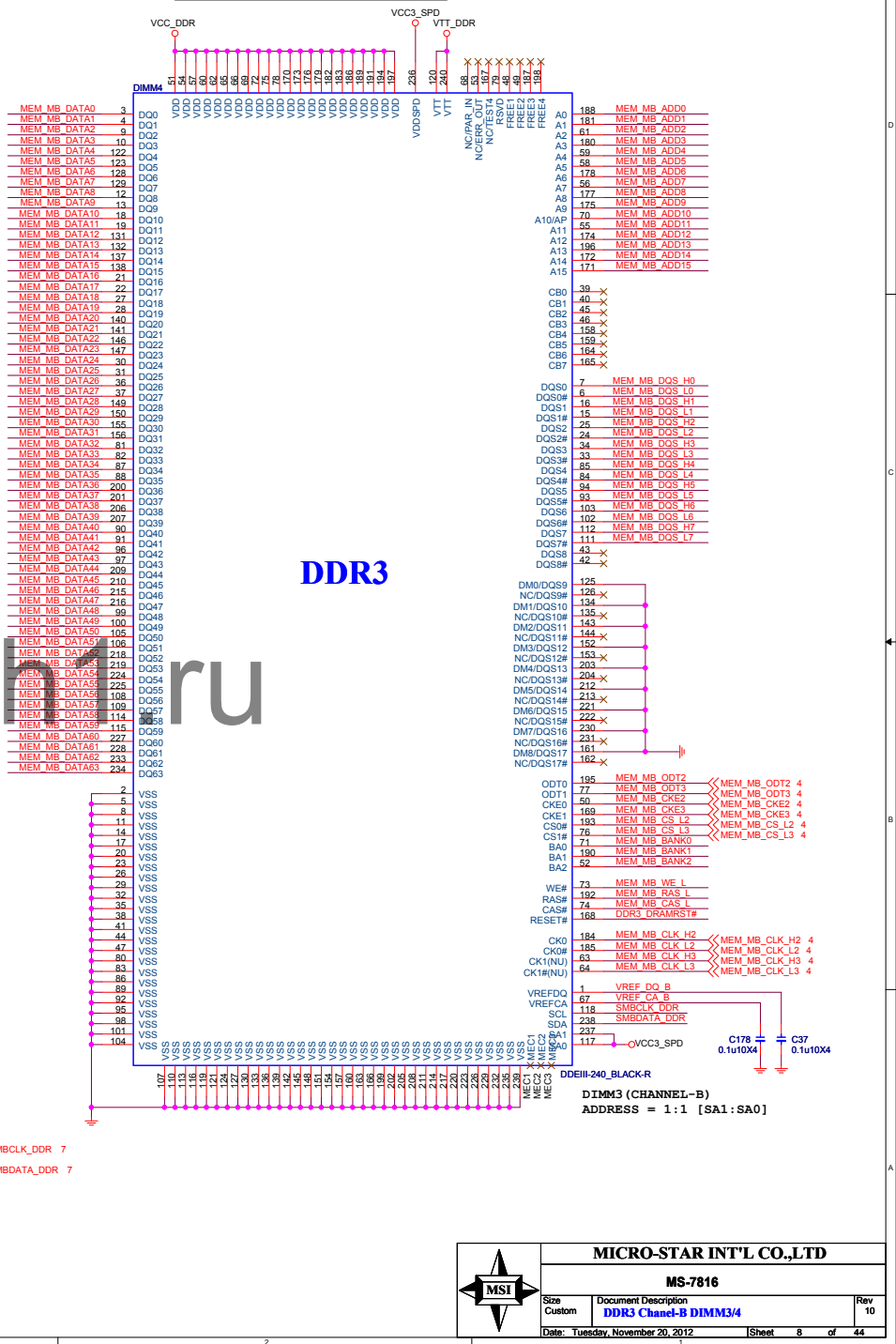


DIMM1 (CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]

DDRIII DIMM_B0



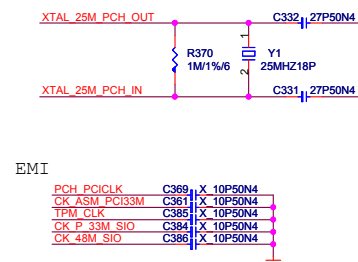
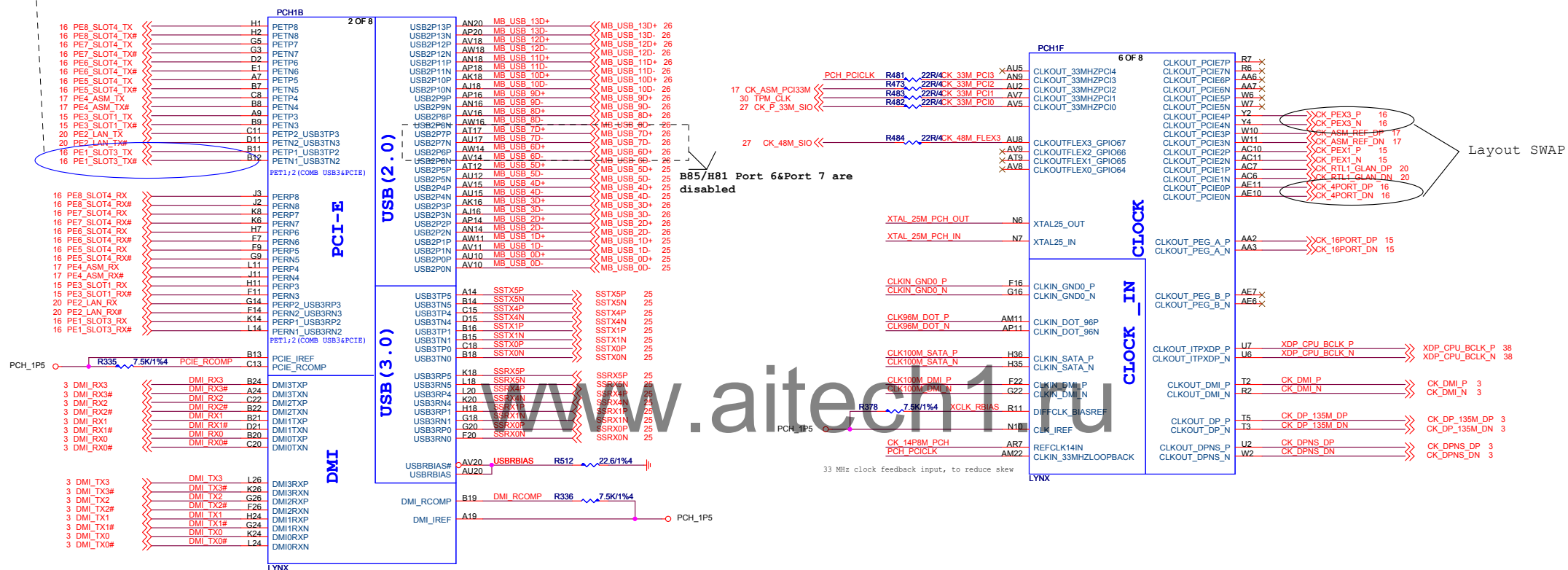
DDRIII DIMM_B1



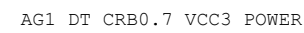
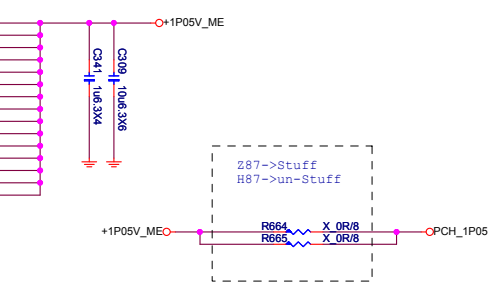
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Size Custom	Document Description DDR3 Chanel-B DIMM3/4	Rev 10
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THE FUTURE

$$(\text{Internal}) \quad 1.29A + (\text{External}) 1.12A = 2.41A$$

$$(\text{Internal})\ 0.261A + (\text{External})\ 0.261A = 0.532A$$


```

Z87->Stuff
H87->un-Stuff

```

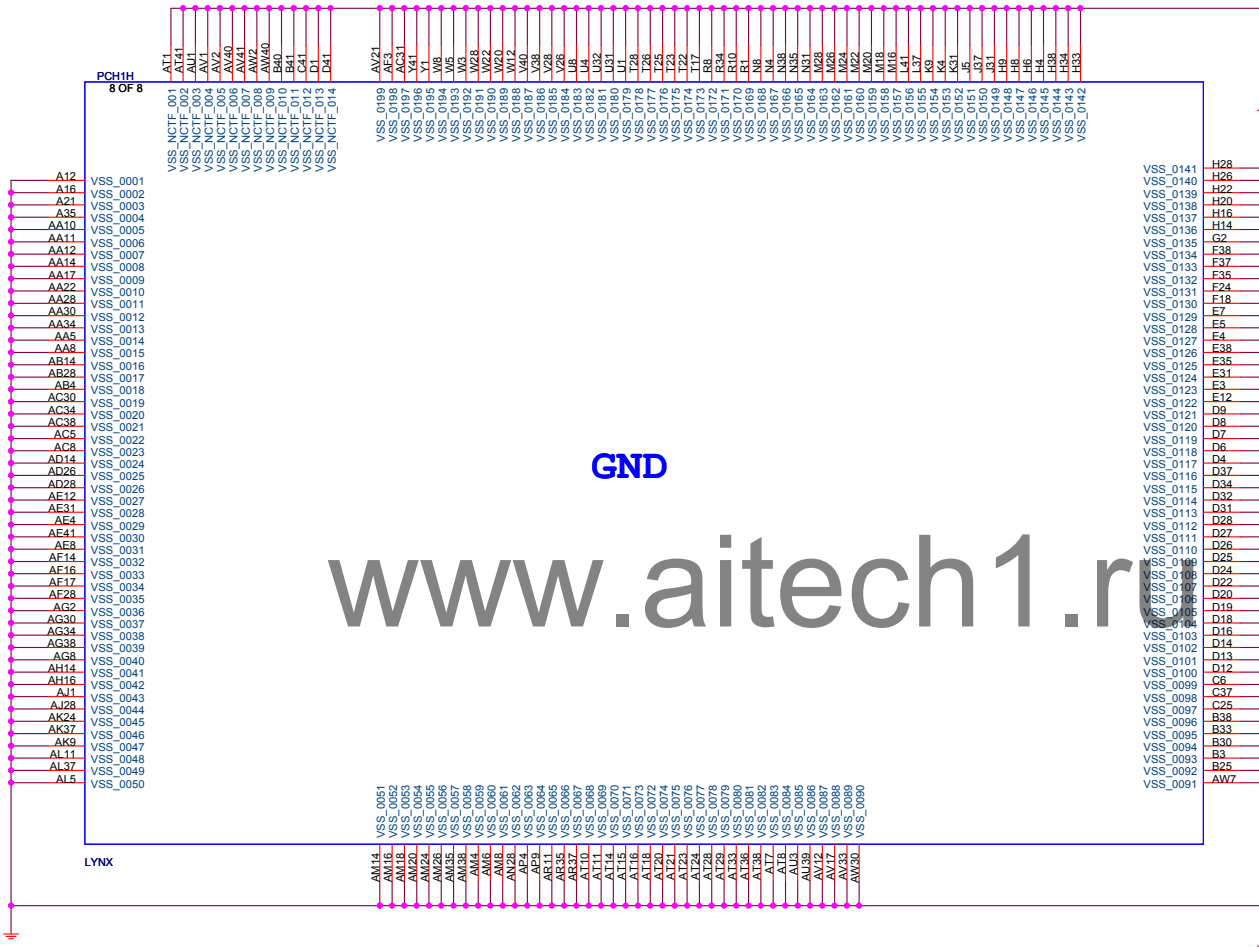
The schematic diagram illustrates the power supply section of the board. It shows the following components and connections:

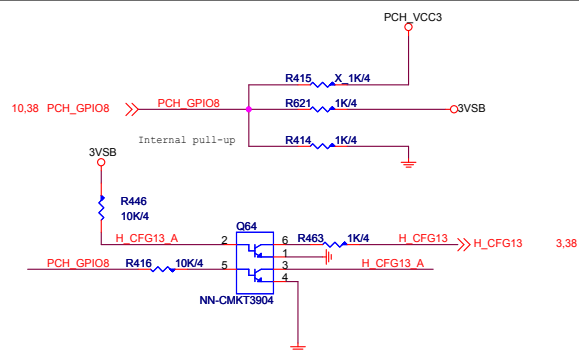
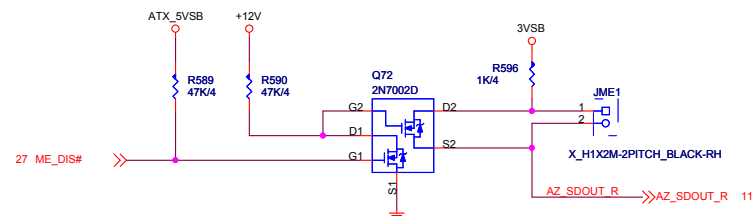
- PCH_1P05** is connected to a network of capacitors: C299 (10uF 3X6), C287 (10uF 3X4), C289 (10uF 3X4), C308 (10uF 3X4), C313 (10uF 3X4), C353 (10uF 3X4), C358 (10uF 3X4), C340 (10uF 3X4), C285 (10uF 3X4), C301 (10uF 3X4), C316 (10uF 3X4), C320 (10uF 3X4), and C334 (10uF 3X4).
- VBAT** is connected to C380 (10uF 3X4) and C389 (0.1uF 10X4).
- 3VSB** is connected to C387 (0.1uF 10X4), C405 (0.1uF 10X4), C389 (10uF 3X4), and C388 (10uF 3X4).
- SPI_VCC3** is connected to C397 (10uF 3X4).
- PCH_VCC3** is connected to C303 (0.1uF 10X4), C389 (10uF 3X4), C347 (0.1uF 10X4), C389 (0.1uF 10X4), C339 (10uF 3X4), C382 (10uF 3X4), C370 (10uF 3X4), C315 (10uF 3X4), and C368 (10uF 3X4).
- PCH_1P5** is connected to C340 (0.1uF 10X4).
- 3VA** is connected to C377 (0.1uF 10X4).



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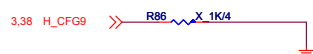




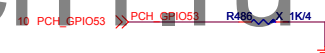
GPI055
Default Mode:
Internal pull-up.

Top Block Swap Mode:
Connect to ground with 4.7k Ohm weak pulldown resistor.

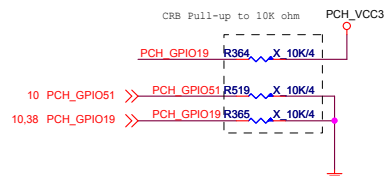
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For Sx power Cycling May Fail Due to SVID Logic Race Condition Within the Processor



GPI053
Connect to ground with 1k Ohm pull-down resistor.



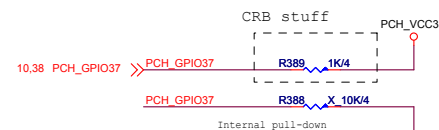
Default (SPI):
Left both SATA1GP/GPIO19 and GPIO51 floating.
No pull up required.

Boot from PCI:
Connect SATA1GP/GPIO19 to ground with 1k
Ohm pull-down resistor.
Leave GPIO51 Floating.

Boot from LPC:
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

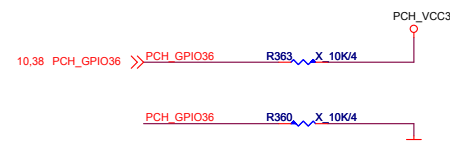
BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1

Default



Enable TLS:
Pull up with 1k Ohm to VccSus3.3.

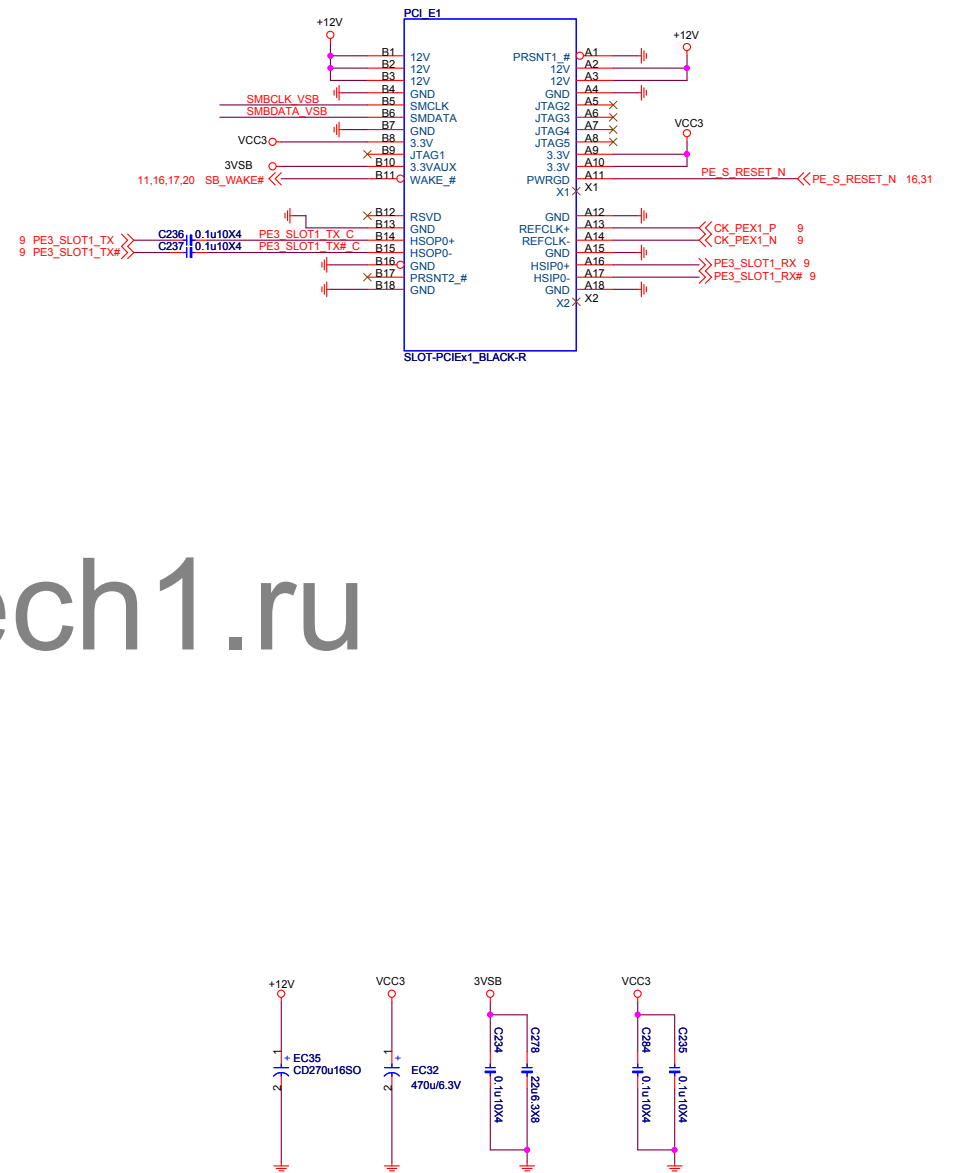
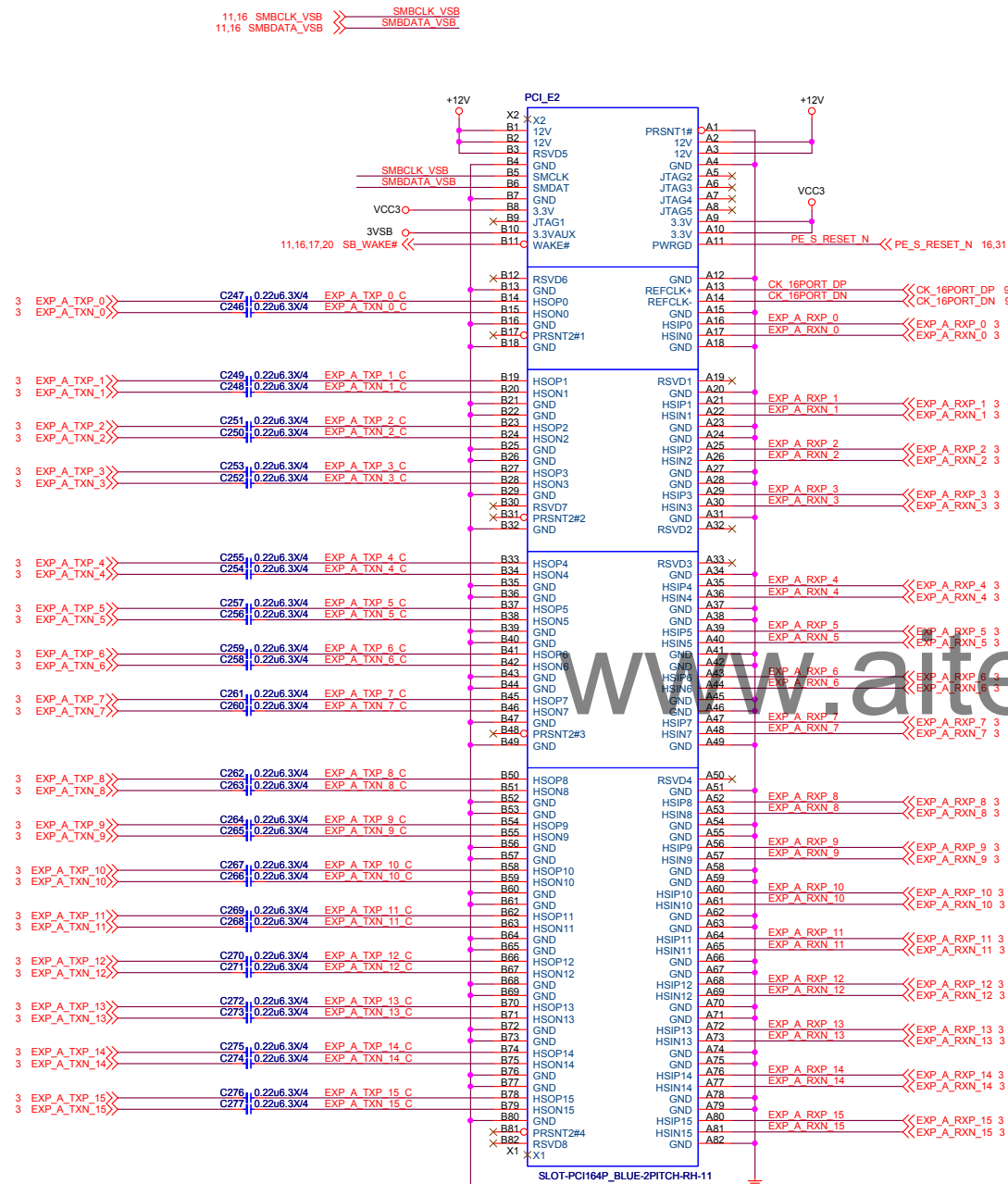
Default (Disable TLS):
Leave NC. Internal pull down.

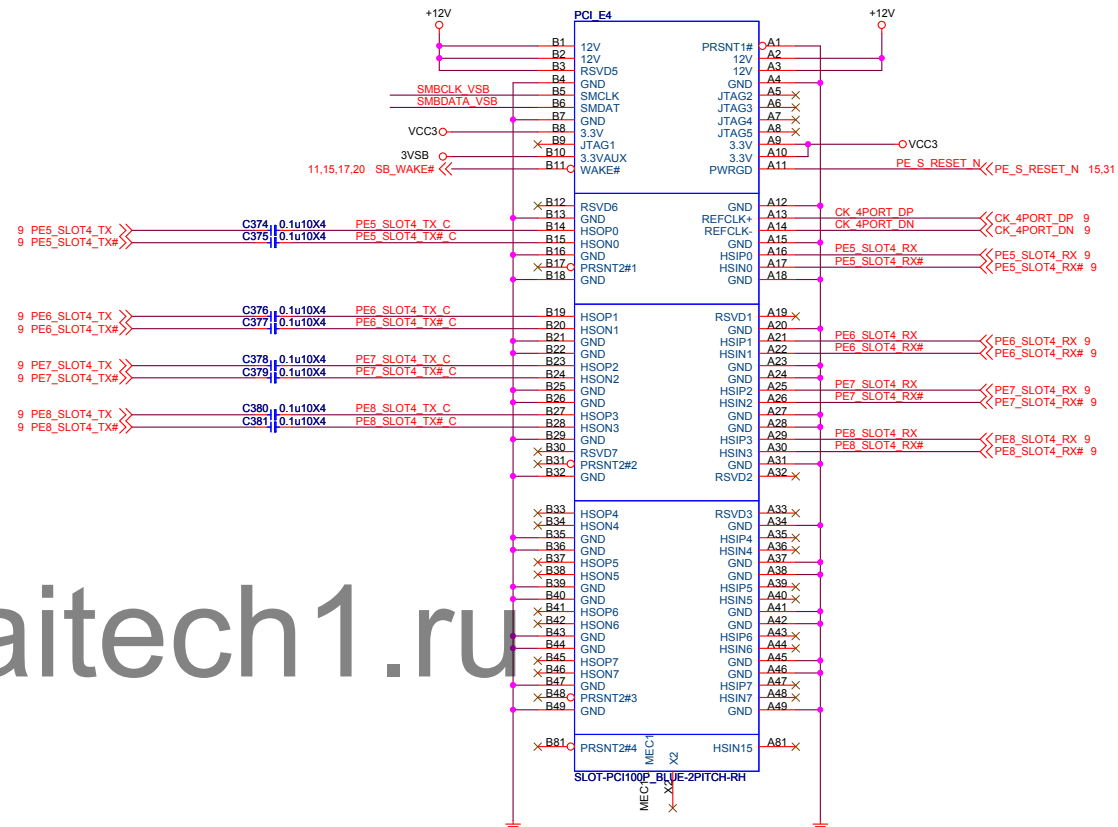


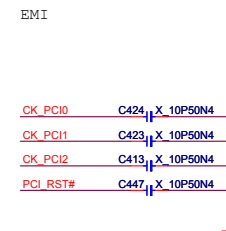
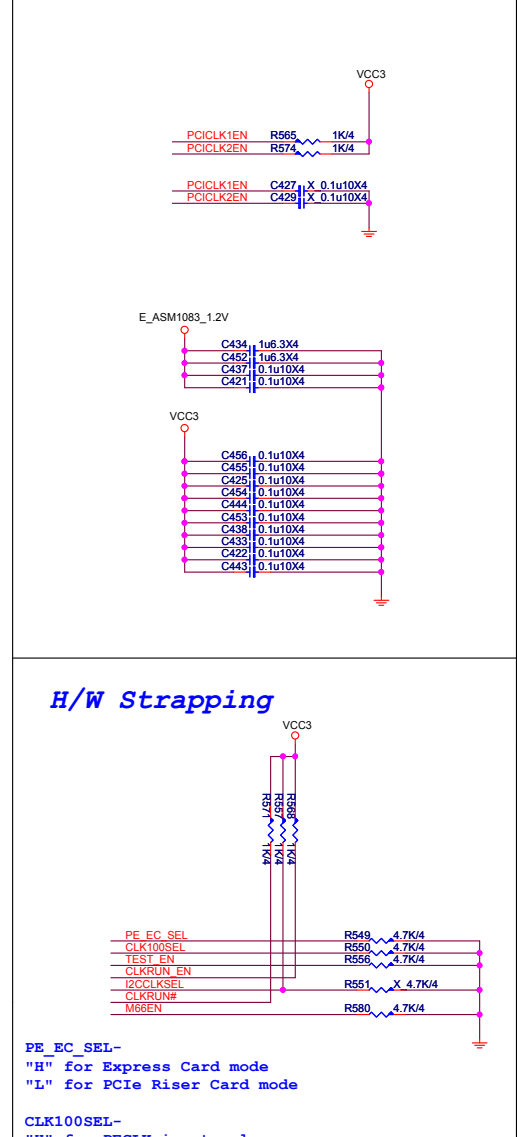
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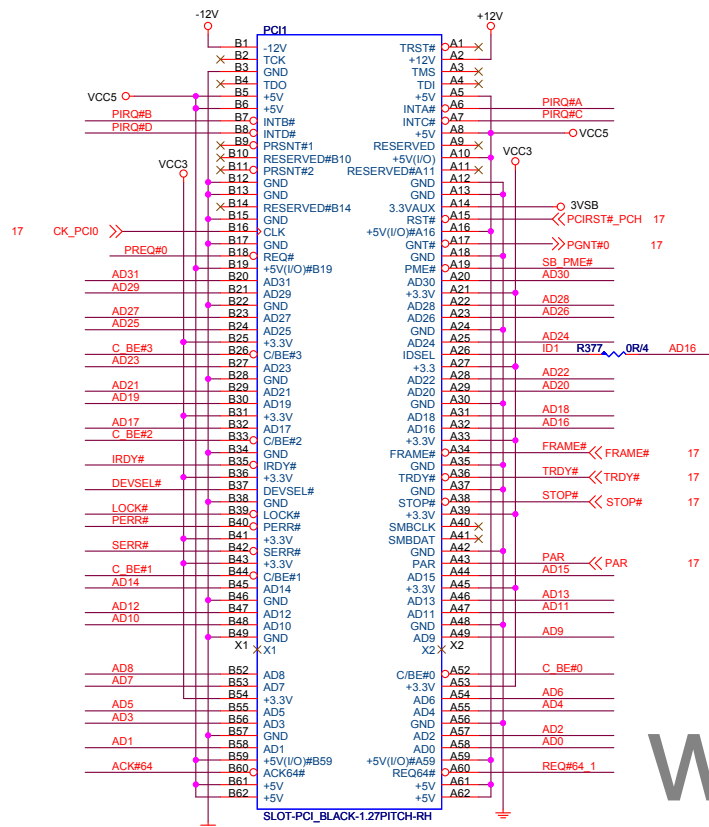
MS-7816

Size Custom	Document Description LYNX-Strap	Rev 10
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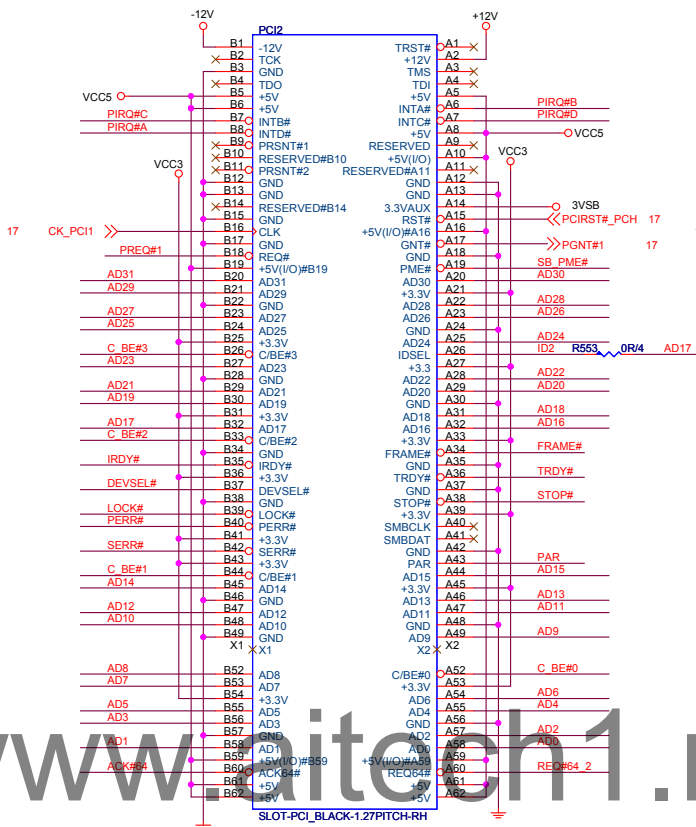




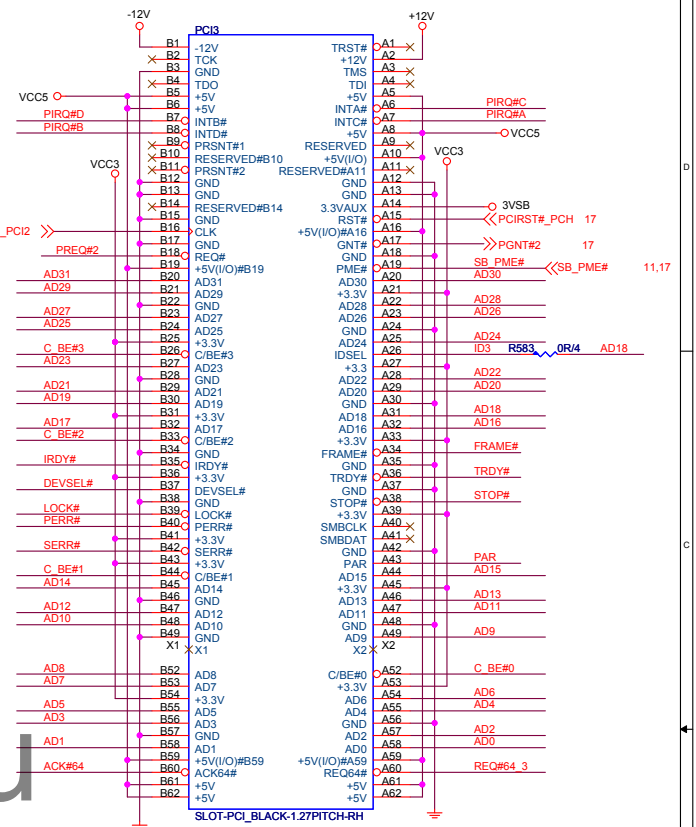




ISDEL = AD16
MASTER = PREQ#0
PIRQ#A



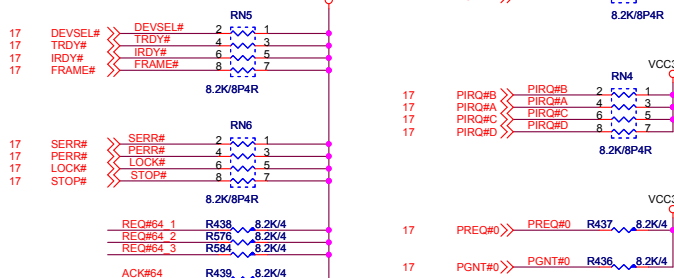
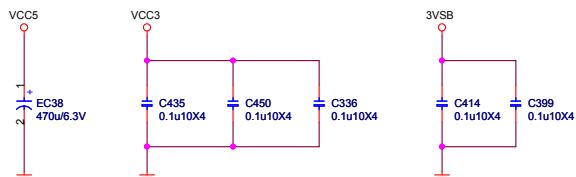
ISDEL = AD17
MASTER = PREQ#1
PIRQ#B



ISDEL = AD18
MASTER = PREQ#2
PIRQ#C

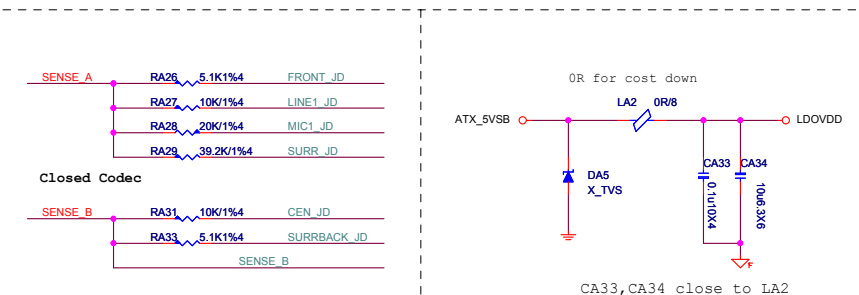
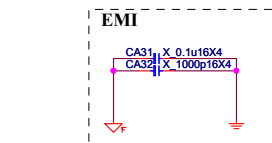
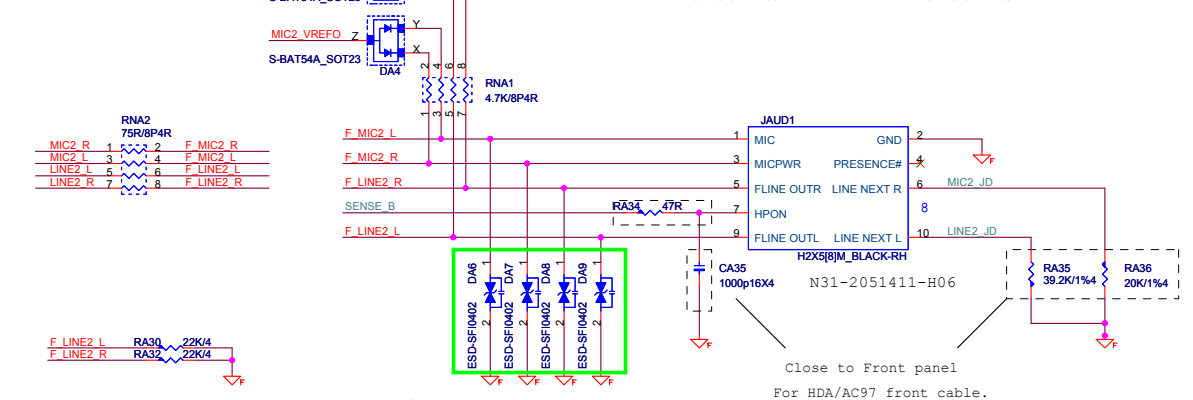
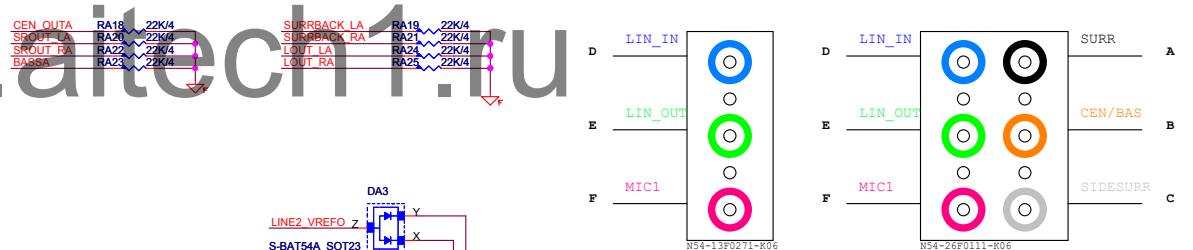
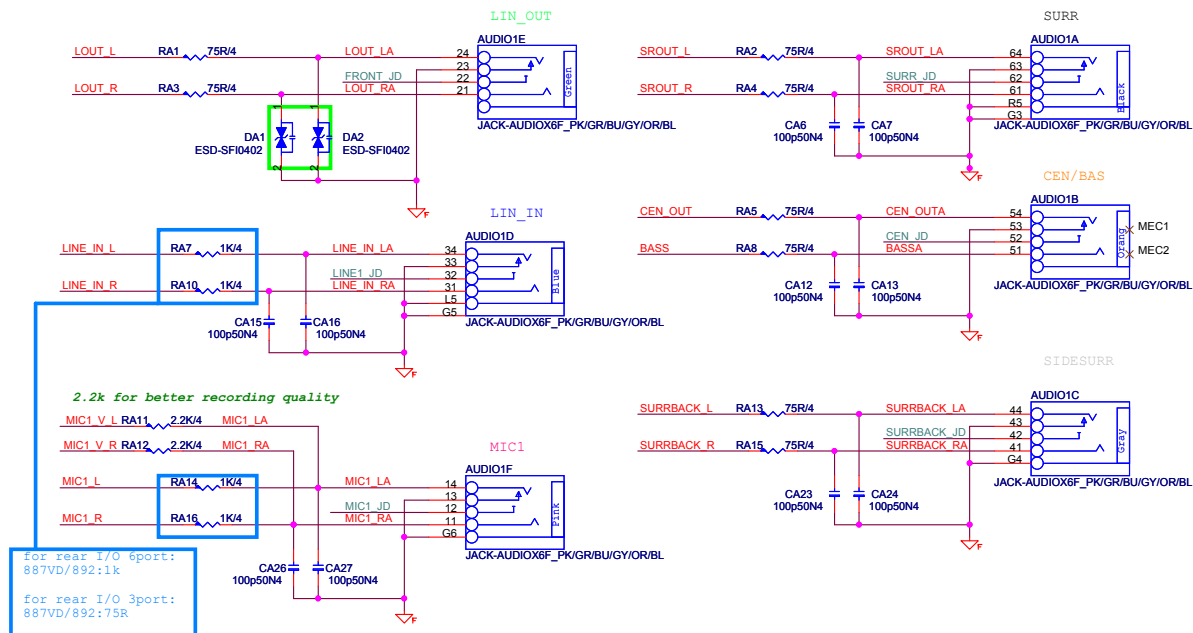
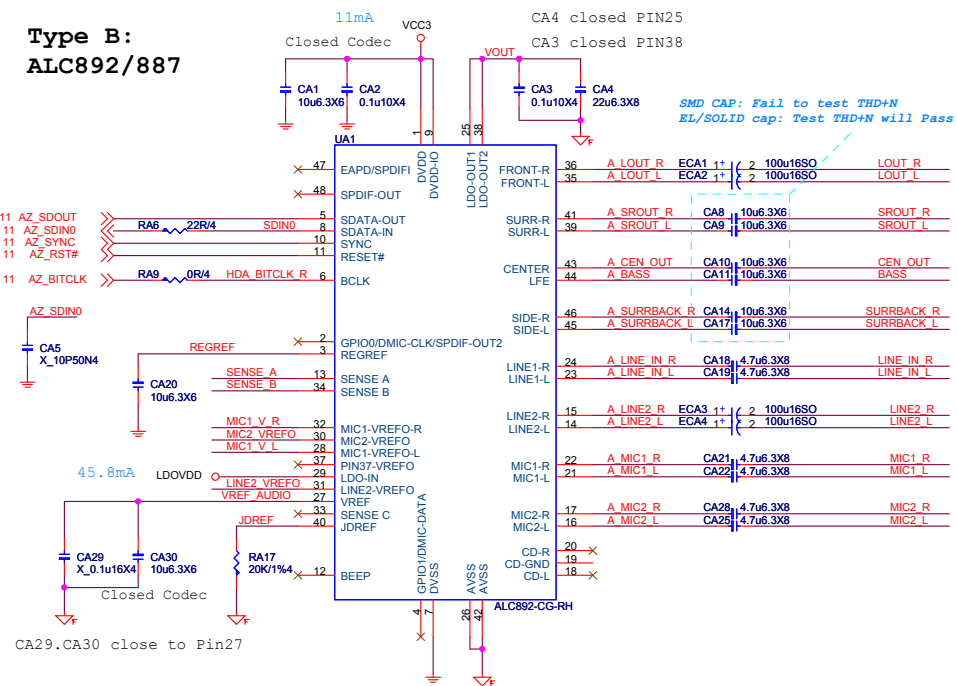
PCI PULL-UP / DOWN RESISTORS

AD[31..0] <<> AD[31..0] 17
C_BE#[3..0] <<> C_BE#[3..0] 17



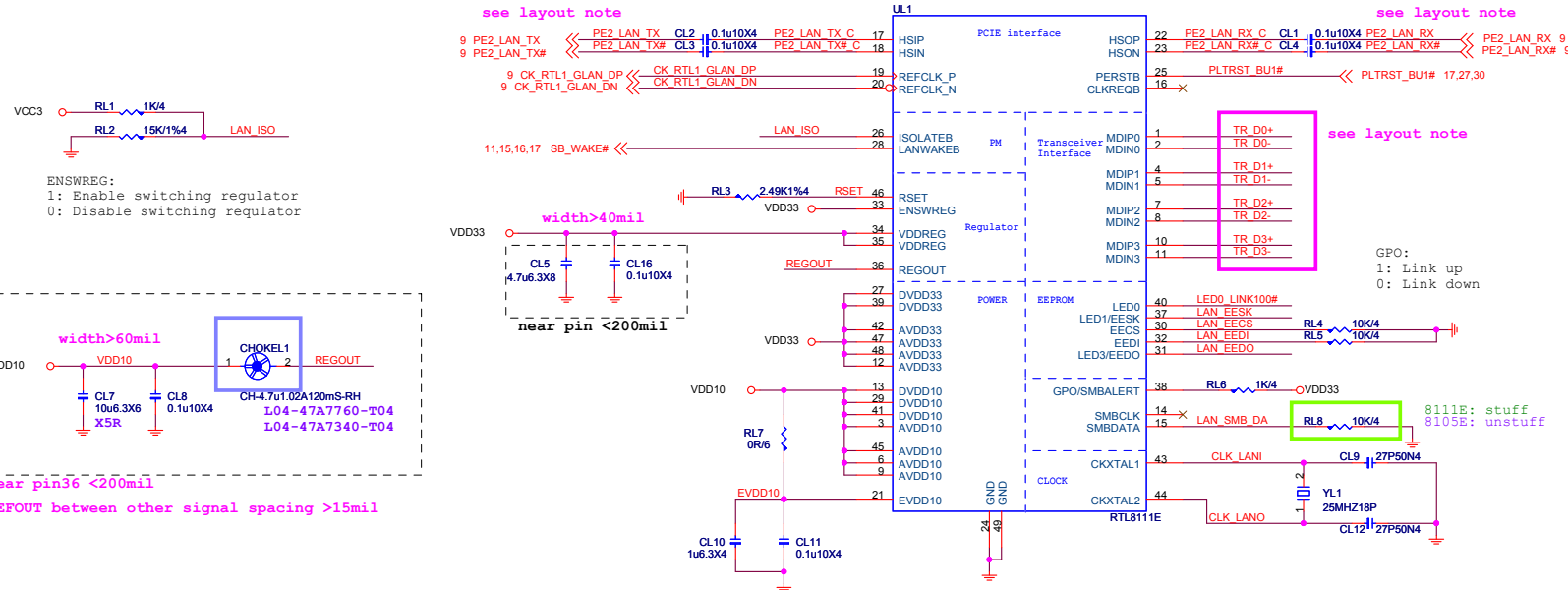
PCI slot (X3)		
+3.3Vaux (wake)	-	1125mA
+3.3Vaux (no wake)	-	60mA
+3.3V	-	7.6A
+5V	-	15A
+12V	-	1.5A

Type B:
ALC892/887



RTL8111E Giga LAN

RTL8105E 10/100M LAN



8111E POWER Consumption

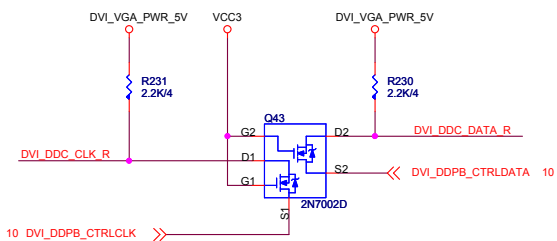
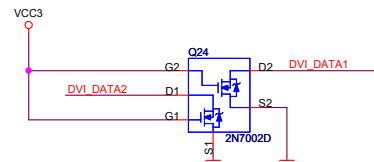
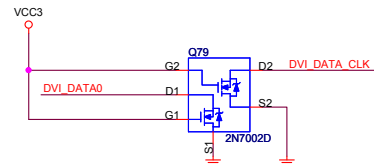
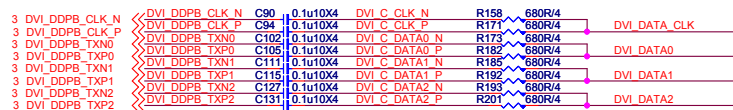
	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

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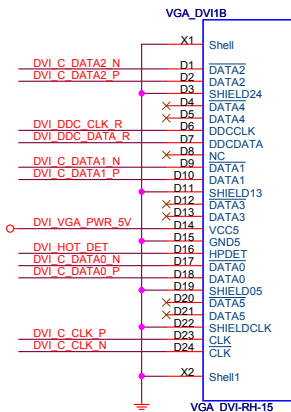
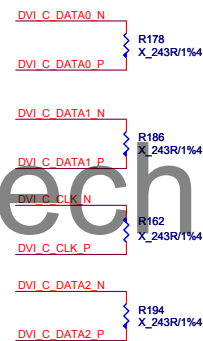
LAN Connector

Giga-Lan	10/100-Lan
N58-22F0731	N58-22F0771
Link Yellow	Link Yellow
Active Blinking	Active Blinking
1000 Orange	1000 Green
100 Green	100 Green
10 None	10 None
19	19
20	20
21	21
22	22

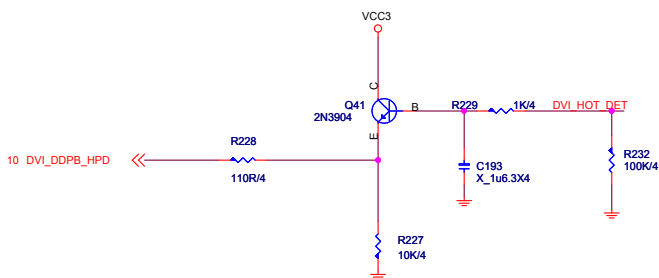
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



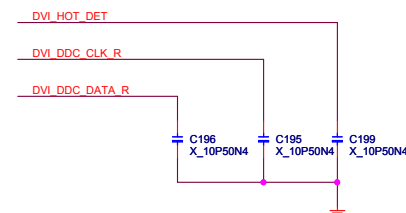
For EMI



HPD



EMI



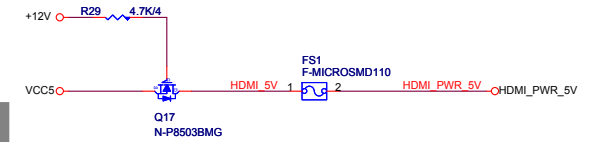
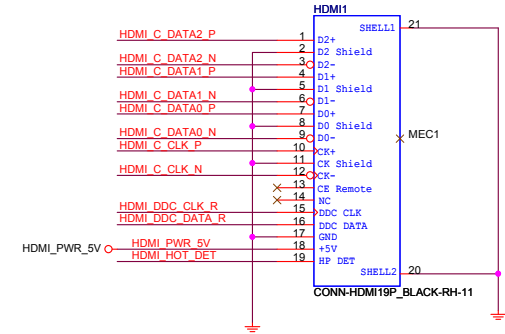
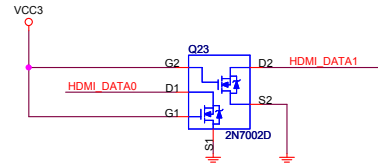
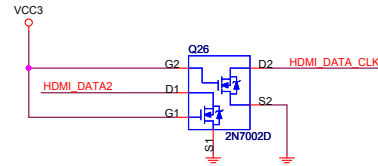
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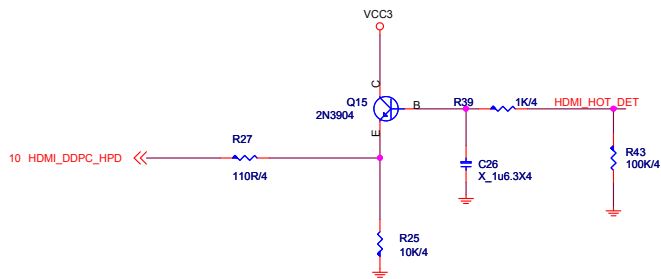
Size	Document Description	Rev
Custom	DVI Connector	10
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HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

3	HDMI_DDPC_CLK_P	HDMI_DDPC_CLK_P	C64	0.1u10X4	HDMI_C_CLK_P	R111	560R/4	HDMI_DATA_CLK
3	HDMI_DDPC_CLK_N	HDMI_DDPC_CLK_N	C66	0.1u10X4	HDMI_C_CLK_N	R115	560R/4	
3	HDMI_DDPC_TX2_P	HDMI_DDPC_TX2_P	C60	0.1u10X4	HDMI_C_DATA2_P	R109	560R/4	HDMI_DATA2
3	HDMI_DDPC_TX2_N	HDMI_DDPC_TX2_N	C58	0.1u10X4	HDMI_C_DATA2_N	R104	560R/4	
3	HDMI_DDPC_TX1_P	HDMI_DDPC_TX1_P	C65	0.1u10X4	HDMI_C_DATA1_P	R112	560R/4	HDMI_DATA1
3	HDMI_DDPC_TX1_N	HDMI_DDPC_TX1_N	C67	0.1u10X4	HDMI_C_DATA1_N	R116	560R/4	
3	HDMI_DDPC_TX0_P	HDMI_DDPC_TX0_P	C61	0.1u10X4	HDMI_C_DATA0_P	R110	560R/4	HDMI_DATA0
3	HDMI_DDPC_TX0_N	HDMI_DDPC_TX0_N	C59	0.1u10X4	HDMI_C_DATA0_N	R105	560R/4	



HPD



For EMI

HDMI_C_CLK_N	R113	X_180R/1%4
HDMI_C_CLK_P		
HDMI_C_DATA0_N	R106	X_180R/1%4
HDMI_C_DATA0_P		
HDMI_C_DATA1_N	R114	X_180R/1%4
HDMI_C_DATA1_P		
HDMI_C_DATA2_N	R108	X_180R/1%4
HDMI_C_DATA2_P		



EMI

HDMI_DDC_CLK_R	C47	X 0.1u10X4
HDMI_DDC_DATA_R	C42	X 0.1u10X4
HDMI_HOT_DET	C38	X 0.1u10X4



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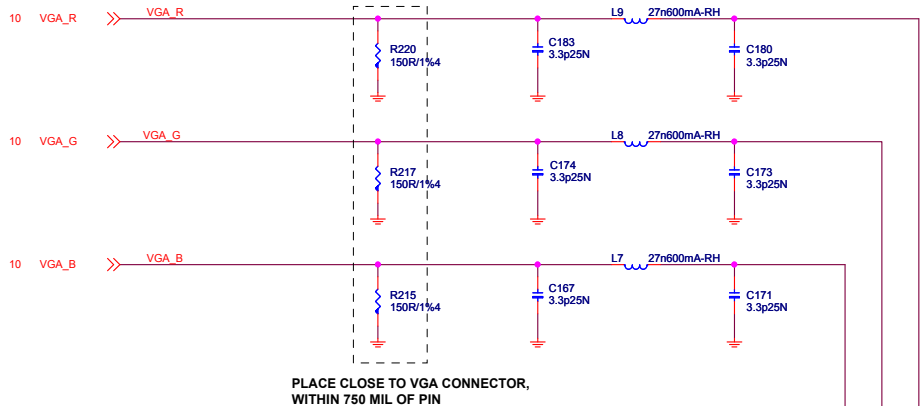
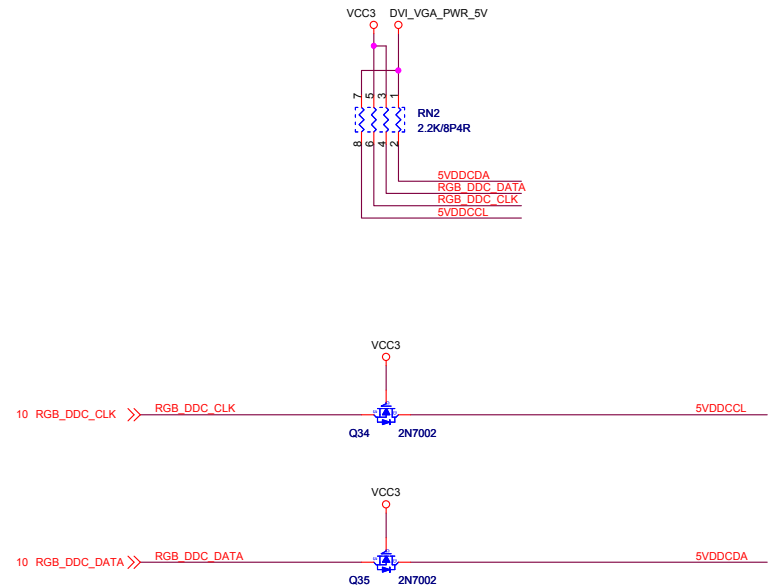
MS-7816

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Custom	HDMI Connector	10
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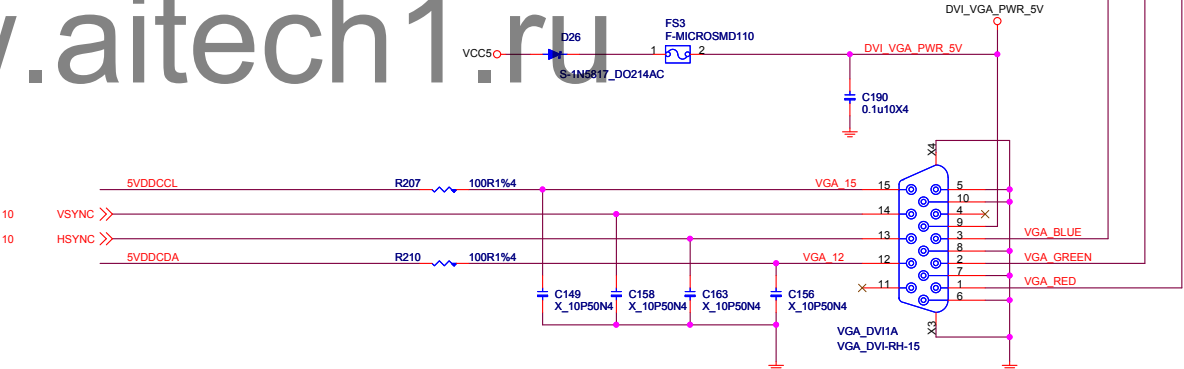
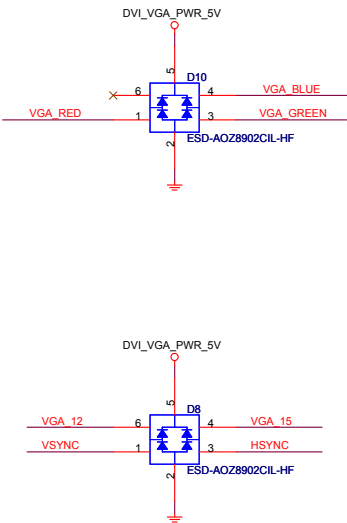
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift



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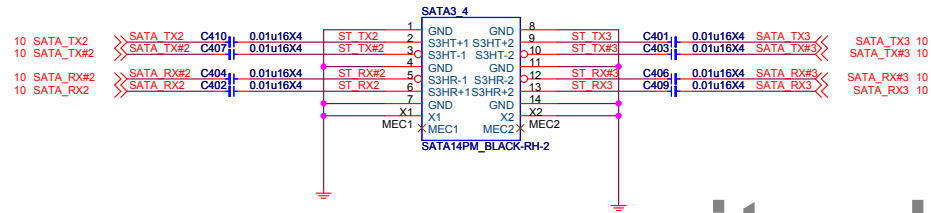
SATA 6G PORT 0,1

3.0



SATA 3G PORT 2,3

3.0

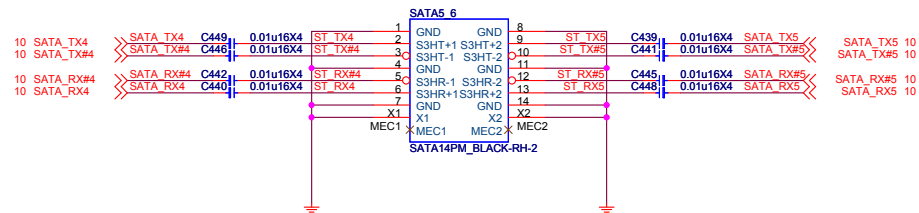


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SATA 3G PORT 4,5

Z87,H87 chip support SATA3.0

B85 chip support SATA2.0



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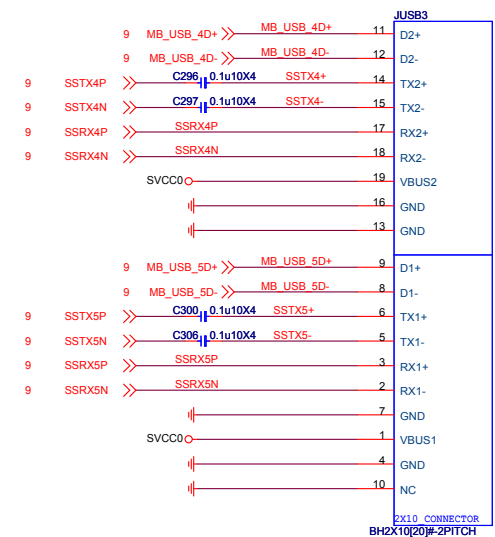
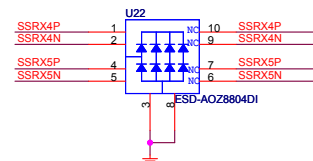
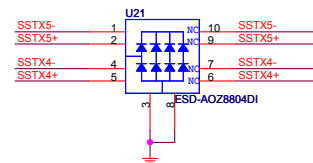
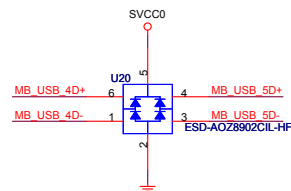
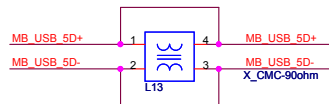
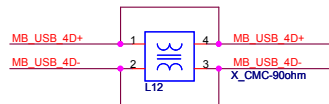
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Size
Custom

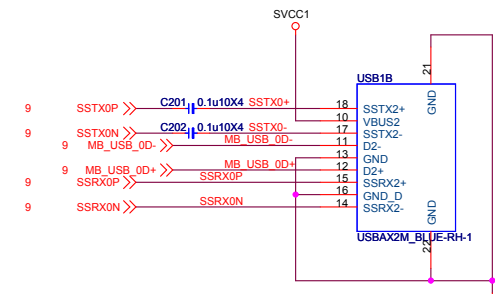
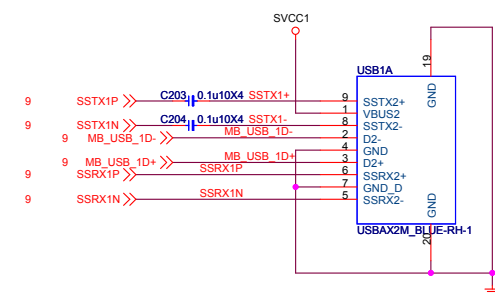
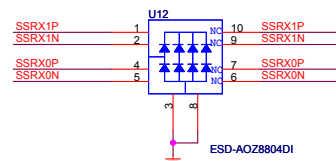
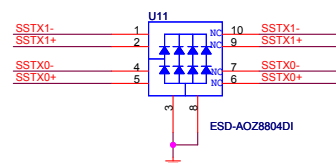
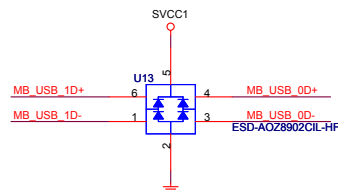
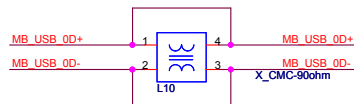
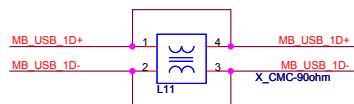
Document Description
SATA Connector

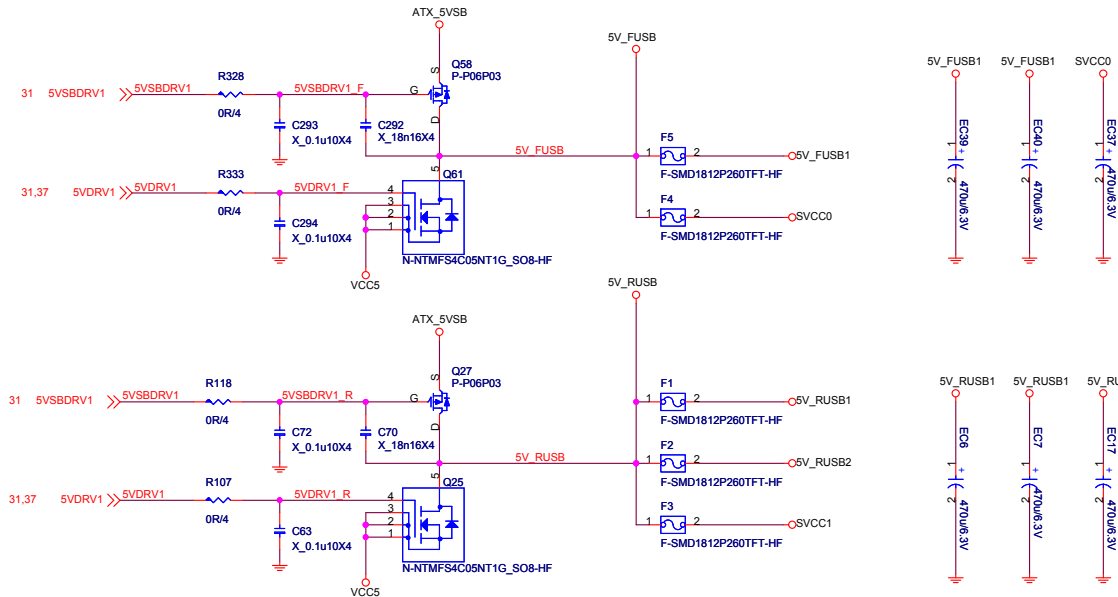
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10

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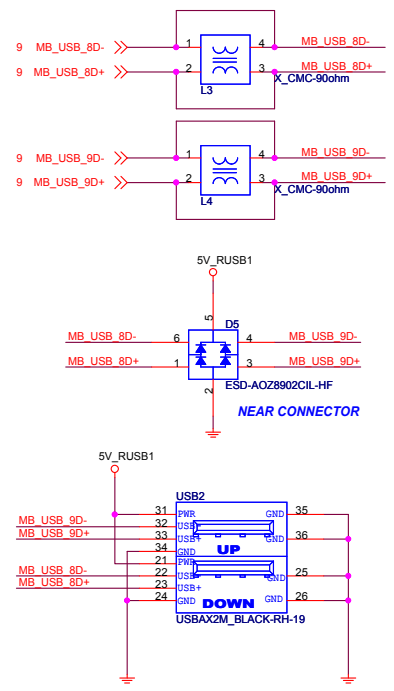
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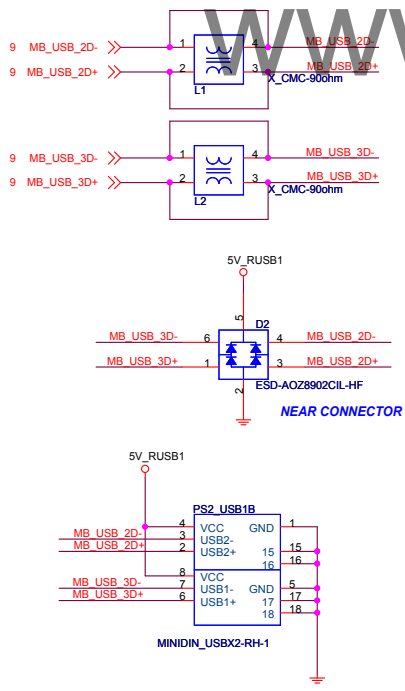


5VDRV1, 5VSBDRV1 width 12mil
D08-0300700-P16 (Itrip=2.6A; 0.015ohm) support 2 USB ports

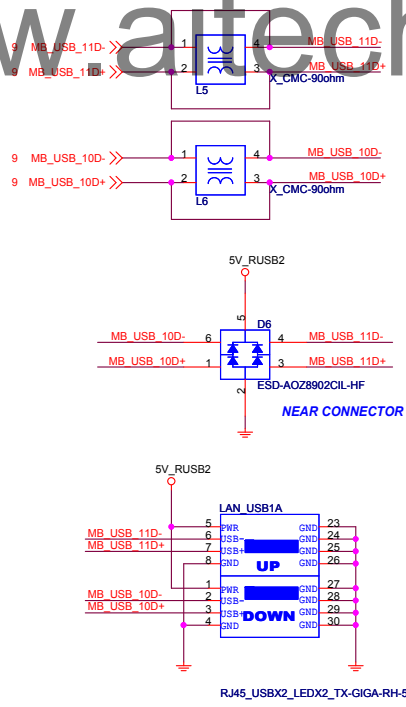
REAR USB PORT 2,3



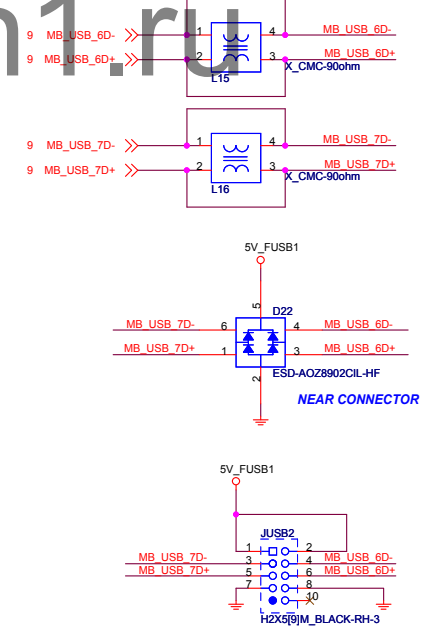
REAR USB PORT 8,9 (With PS2)



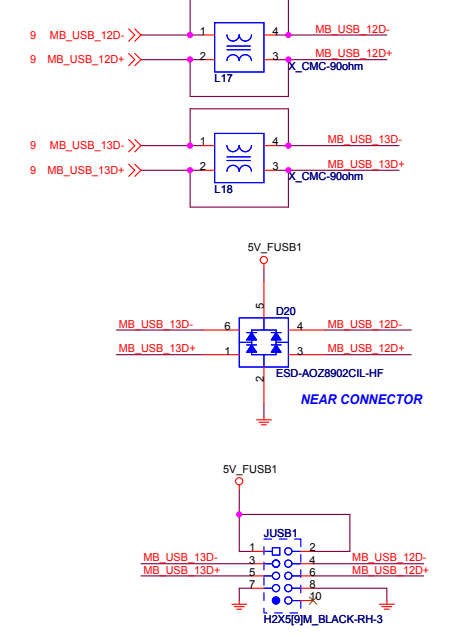
FRONT USB PORT 10,11 (With LAN)

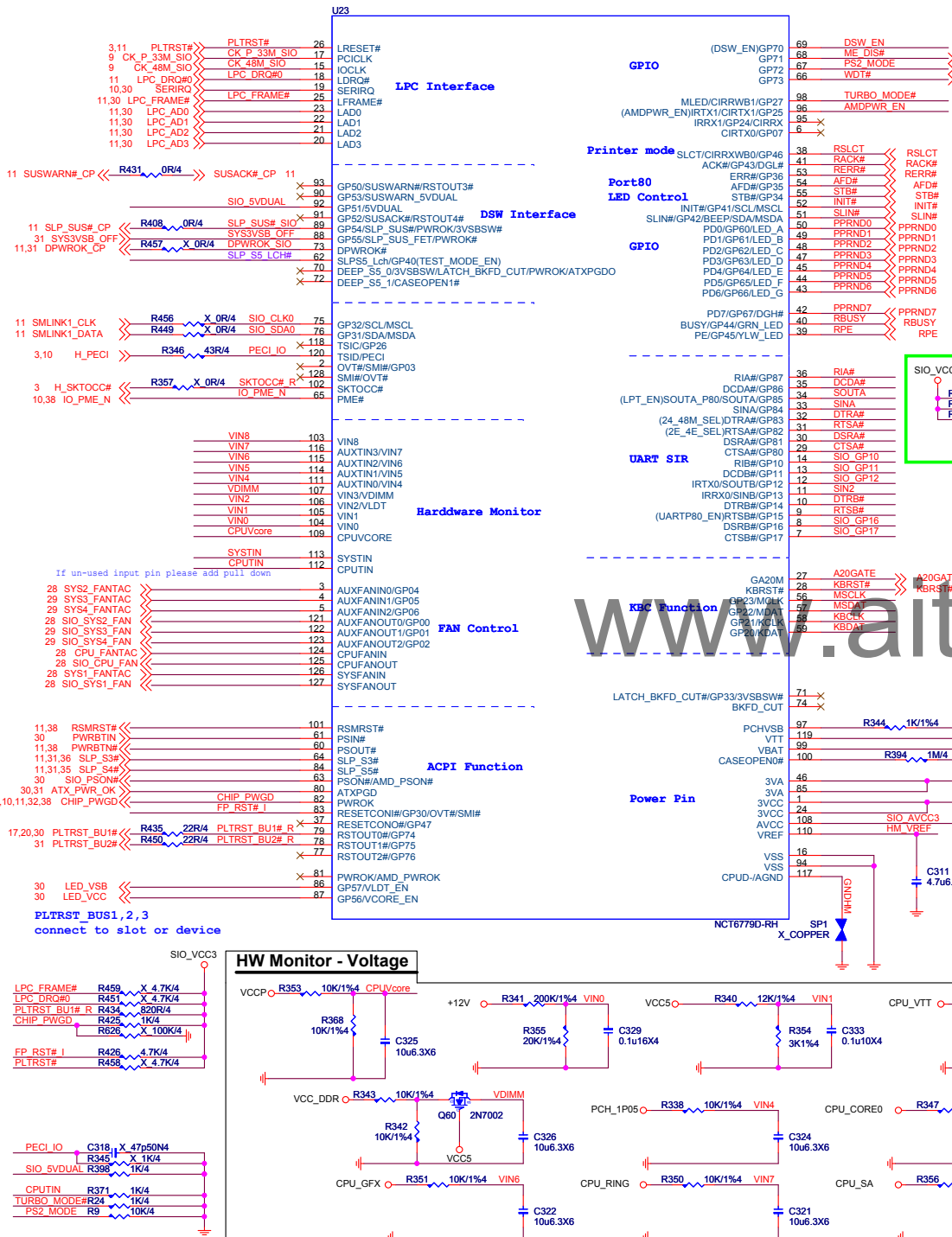


FRONT USB PORT 6,7

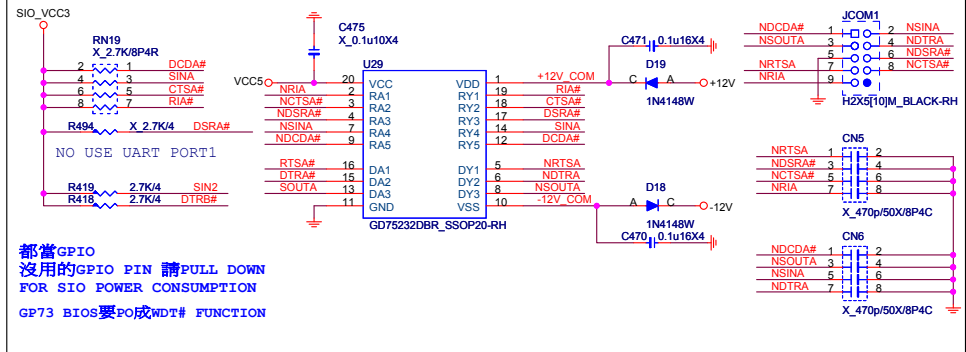


FRONT USB PORT 12,13



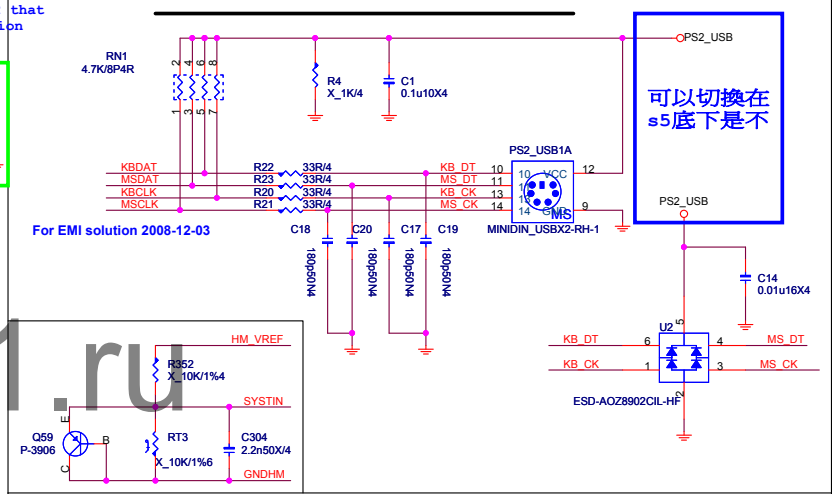


SERIAL PORT 1

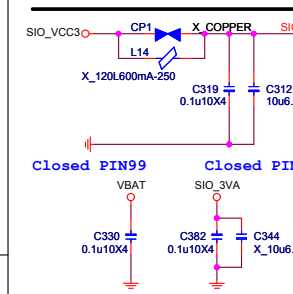


都當GPIO
沒用的GPIO PIN 請PULL DOWN
FOR SIO POWER CONSUMPTION
GP73 BIOS要PO成WDT# FUNCTION

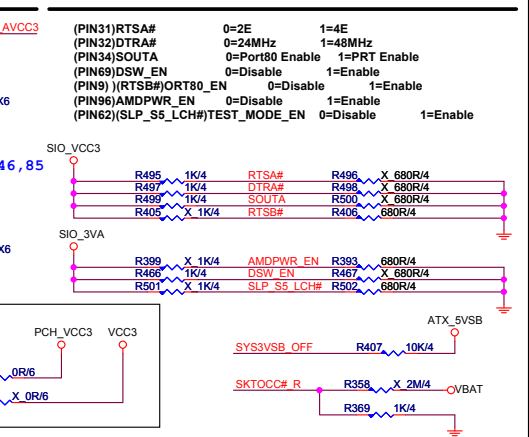
PS2 KEYBOARD & MOUSE CONNECTOR



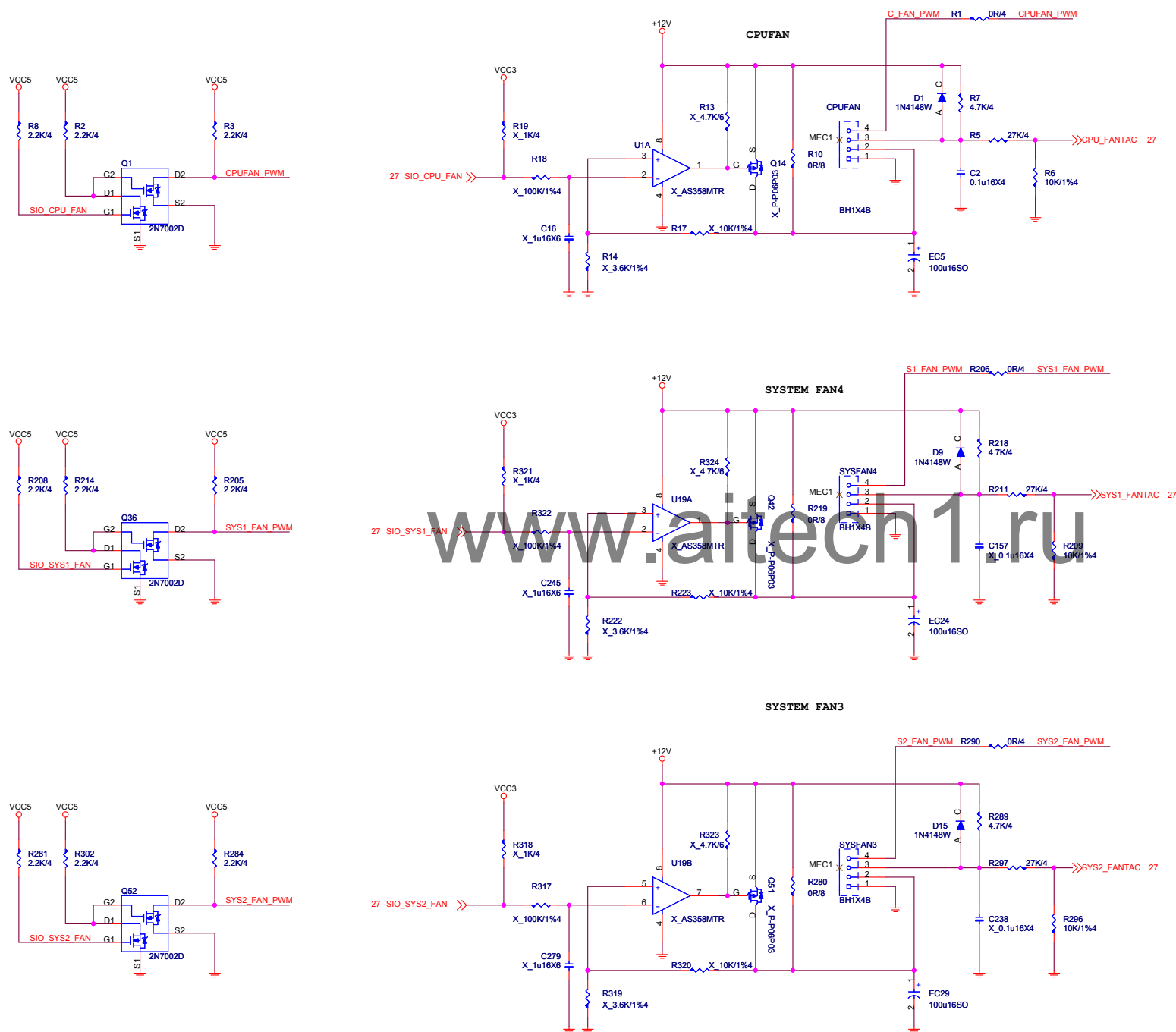
3V Analog Power



SIO Pin Strap



FAN-COUNTROL CIRCUIT

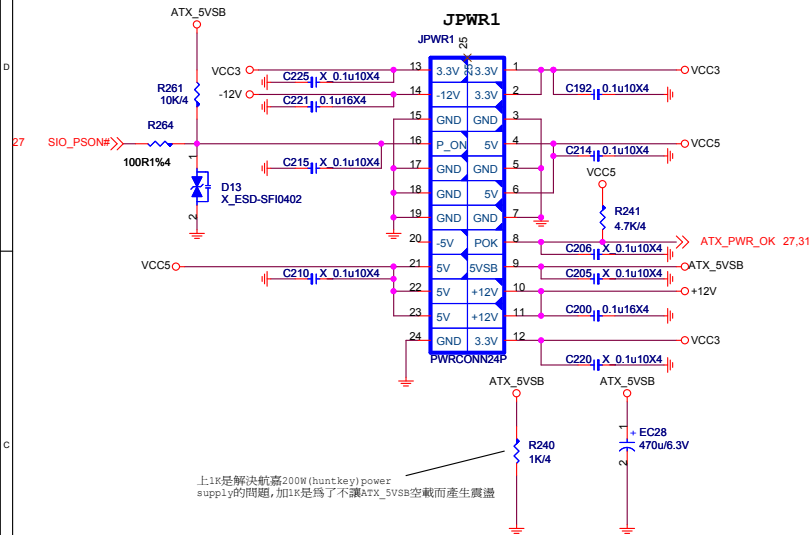


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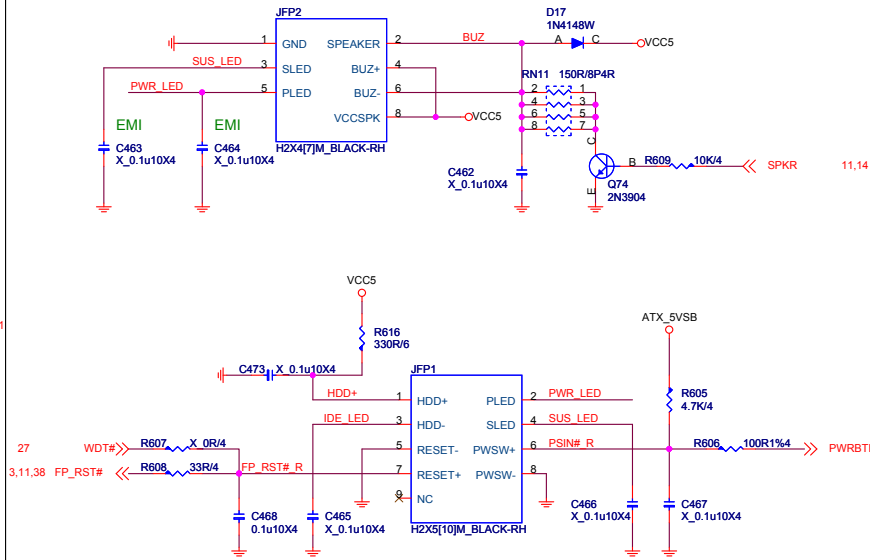
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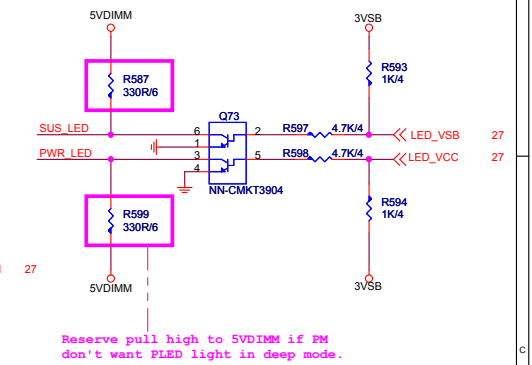
ATX POWER CONNECTOR



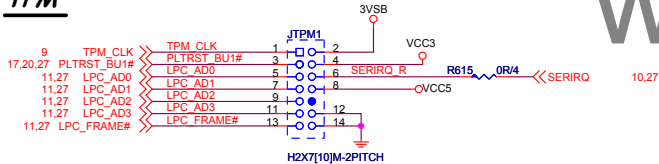
FRONT PANEL



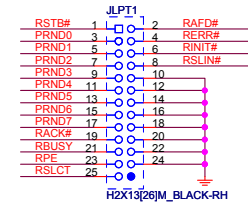
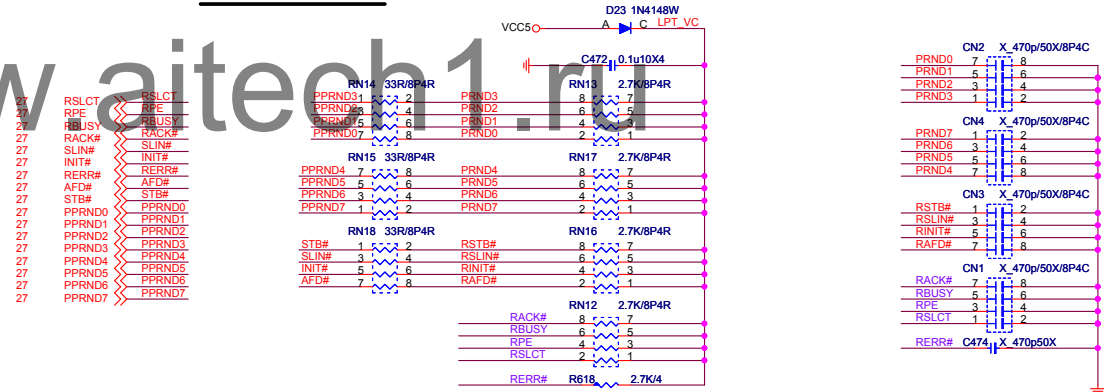
LED (for Fintek 71869)



TPM



PARALLAL PORT



N31-2131151-H06 : 2.0mm
N31-2131131-H06 : 2.54mm

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Custom	ATX F_Panel/EMI/TPM	10	
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5V DIMM FOR DDR

VCC5 ○ R77 510R/4 5V DIMM_5V R89 10K/4 5V DIMM_5V R82 10R/4 ATX_5VSB C45 0.1u10X4

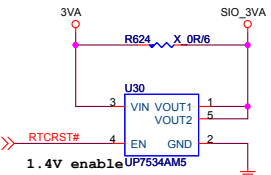
27.30 ATX_PWR_OK >> 5V DIMM_5V 5V DIMM_5V 5VSB_DRV 7 5VSBDRV1 C48 18n16X4 P-P06P03 Q76

11.27.36 SLP_S3# >> 5 5VCC 5VSB 5VCC_DRV 8 5VDRV1 R91 1K/1%6 C51 0.022u16X4 Q77 N-P0903BKB_PDFN8-HF

11.27.35 SLP_S4# >> 6 5VCC 5VSB 5VCC_DRV 8 5VDRV1 R91 1K/1%6 C51 0.022u16X4 Q77 N-P0903BKB_PDFN8-HF

7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

26 5VSBDRV1 << 5VSBDRV1
26.37 5VDRV1 << 5VDRV1



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[illegible]

GPIO13 from PCH

TO ALL PCIE SLOT RESET#

VCC3

C400
X_0.1u10X4

U25

11 PCH_GPIO13 >> PCH_GPIO13

27 PLTRST_BU2# >> PLTRST_BU2#

4 >> PE_S_RESET_N 15,16

X_NC7SZ08M5X_SOT23-5

R535 0R/4

PCIE_SLOT_RESET_N
from SIO_RESET_BUS2

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DDR Power:1.5V

DDR3_1.5V 4.2A+12A+1.115A+6A=23.315A

4.2A FOR CPU

12A FOR 4DIMM

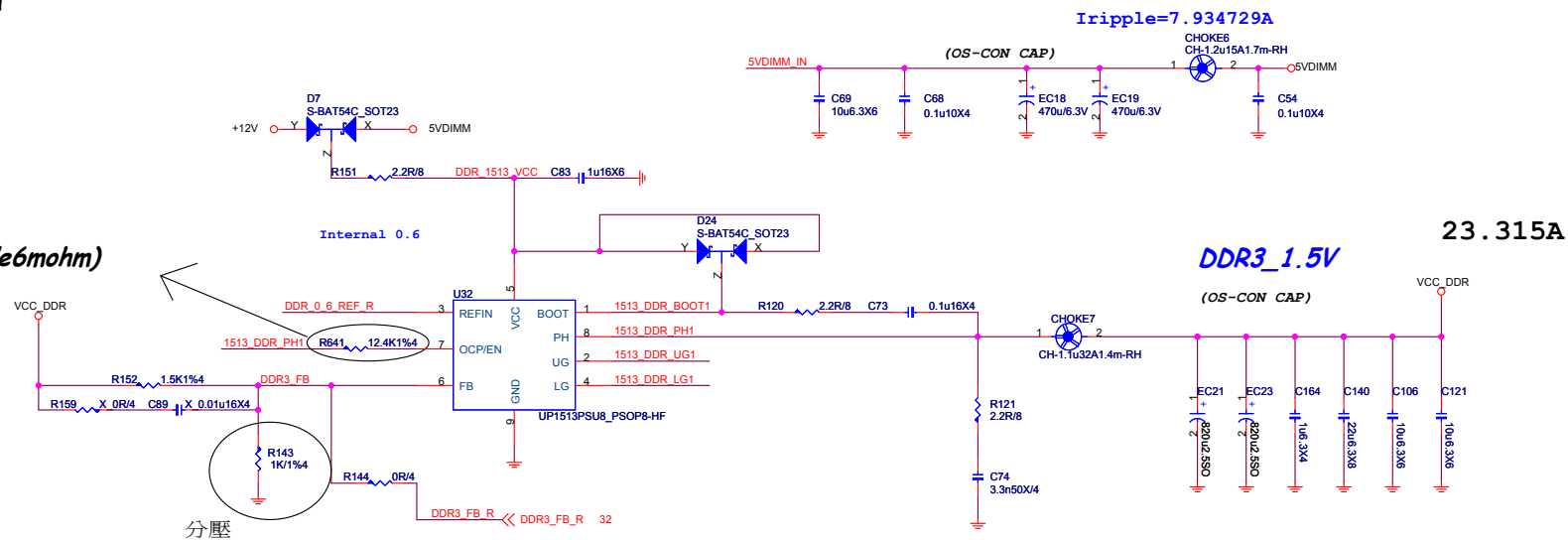
1.115A FOR VTT_DDR

PCH Core 6A

OCP 23.315*1.5=35A

35A=(40uA*Roccs(R641)-0.4V)/Rdson(Low side6mohm)

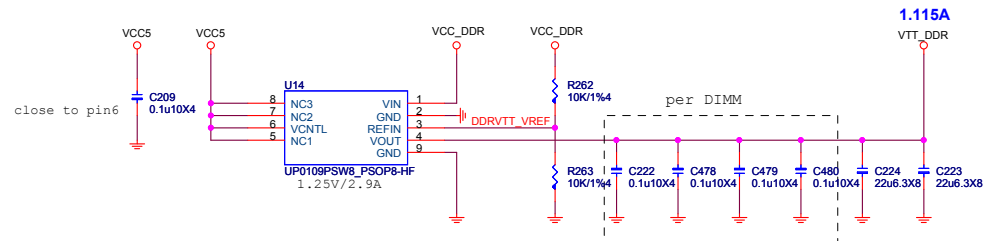
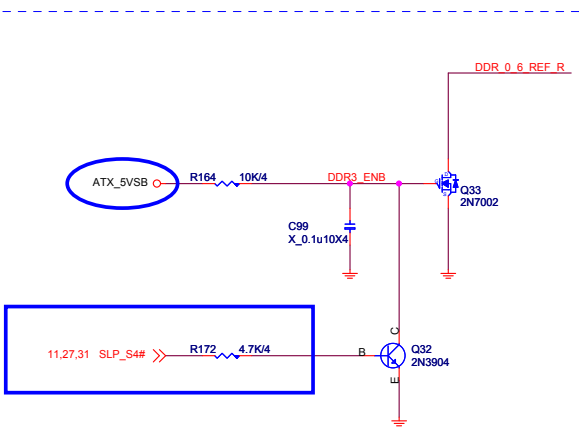
R641=12.4K ohm



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DDR VTT Power

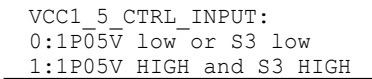
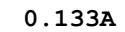
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



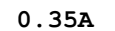
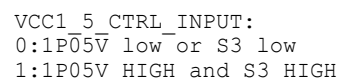
MICRO-STAR INT'L CO.,LTD			
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Custom	DDR Power -UP1513 - DDR POWER	10	
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P.S. Only for meet Intel power down sequence.

PCH Core 6A



Waitting PCH_1P05 Ready

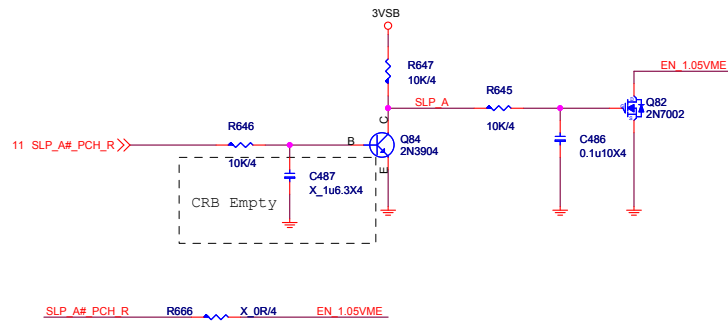


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Size Custom	Document Description PCH Power - uP1513 1-Phase MOS		Rev 10
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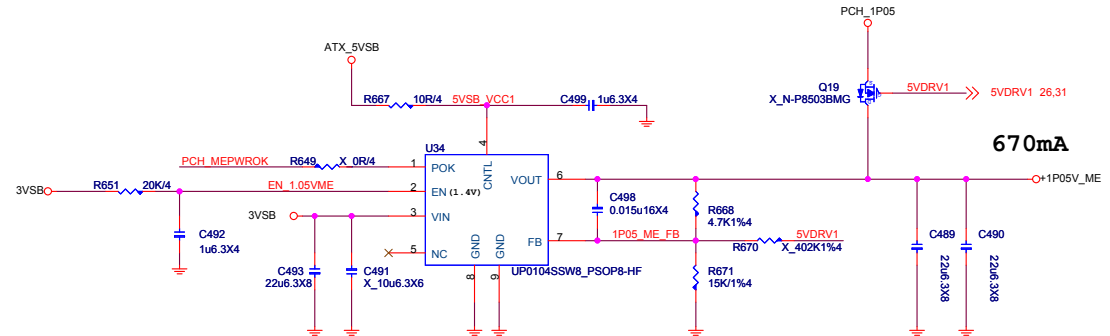
C318,C323,R378,C313,C314,C333,R366 for H87 un stuff
Z87 only stuff R354

SLP_A

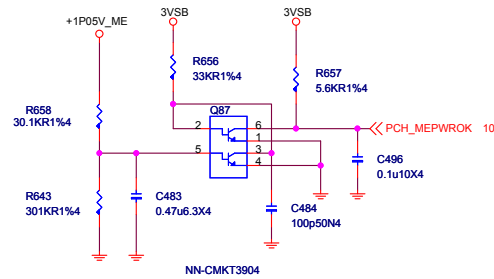
ME Power Control



+1.05V_ME(VCCIO_ME)



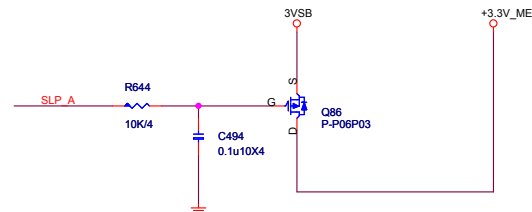
PCH_MEPWROK



VccASW active to APWROK high 1ms

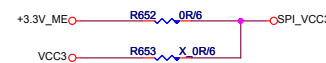
APWROK falling to VccASW falling 40ns

+3.3V_ME



For INTEL ME BUG

Z87->Stuff R366
H87->Stuff R354

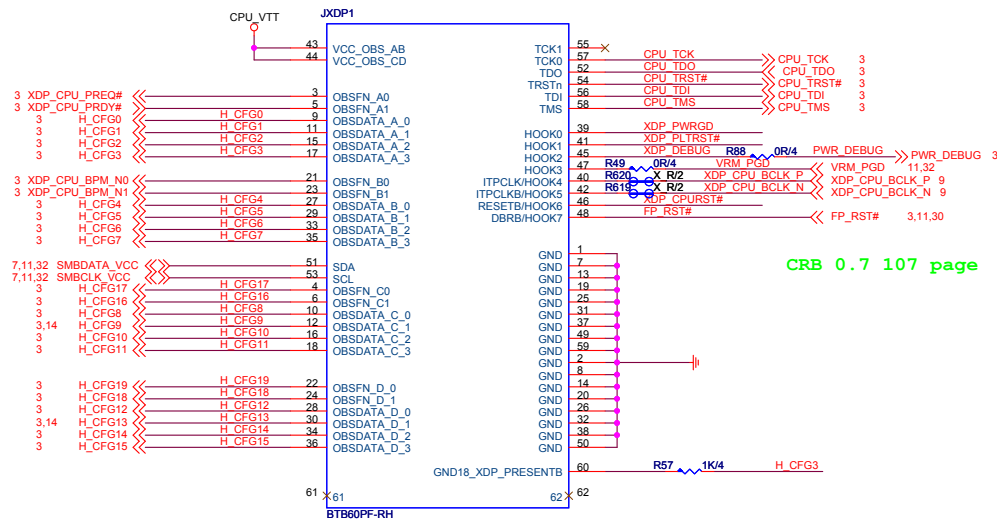


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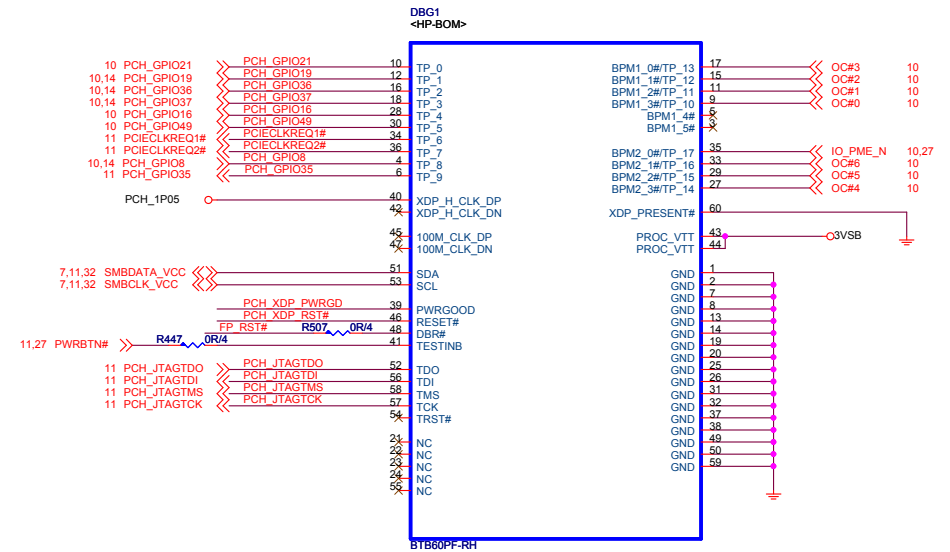
MS-7816

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Reserve debug port 5020

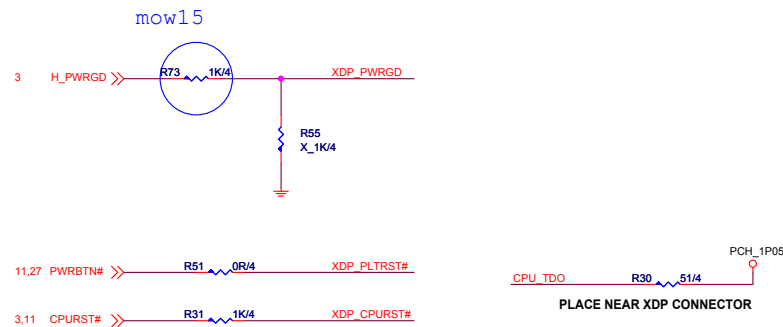


PCH XDP



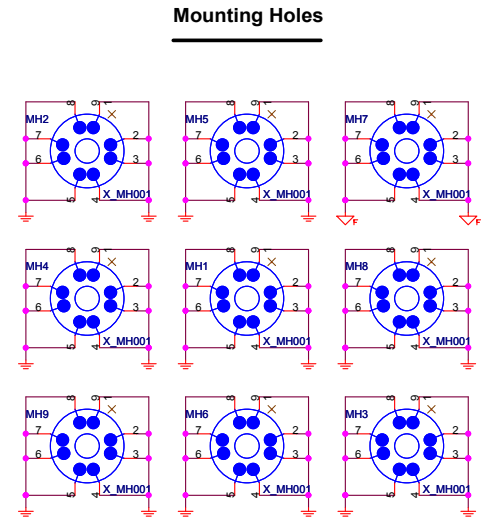
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PCH XDP PWRGD/RESET





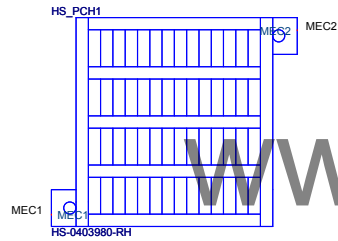
2012/11/162012/11/23PK0-0781610-G37, 精成, 23, 寶安恩斯邁廠 (MSIS) 4, Coffee
2012/11/162012/11/23PK0-0781610-G37, 精成, 27, 寶安恩斯邁廠 (MSIS) 4, Coffee
2012/11/162012/11/23PK0-0781610-E48, 競華, 23, 寶安恩斯邁廠 (MSIS) 4, Coffee
2012/11/162012/11/23PK0-0781610-E48, 競華, 27, 寶安恩斯邁廠 (MSIS) 4, Coffee



Test point

VCCP	○	□	VCCP
VCC_DDR	○	□	VCC_DDR
VTT_DDR	○	□	VTT_DDR
PCH_1P05	○	□	PCH_1P05
PCH_1P5	○	□	PCH_1P5
5VDIMM	○	□	5VDIMM
3VSB	○	□	3VSB
VBAT	○	□	VBAT
3VA	○	□	3VA
PCH_VCC3	○	□	PCH_VCC3
CPU_VTT	○	□	CPU_VTT

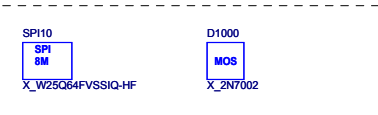
HEATSINK



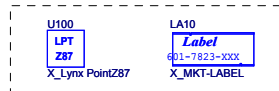
H87 OPT.



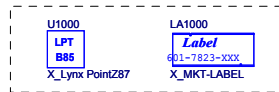
SPI OPT.



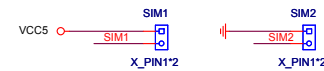
Z87 OPT.



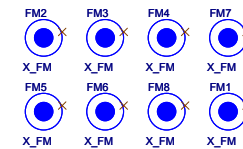
B85 OPT.

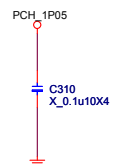
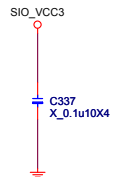
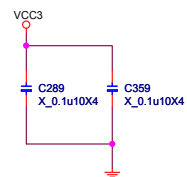
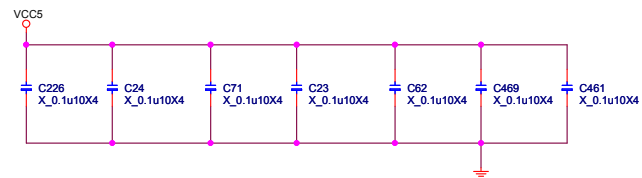


Simulation



Optical Fiducial Marks-120





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